Ordering number : EN7814D

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LA6242H — Monolithic Linear IC For CD Player 4-channel Bridge (BTL) Driver

Overview

The LA6242H is a 4-channel motor driver IC for home and car CD players. It provides a pin for switching the channel 1 input.

Functions

- Four bridge-connected (BTL) power amplifier circuits
- I_O max: 1A
- Built-in level shifter circuits
- Muting circuit (on/off control for all outputs)
- High output voltage (dynamic range): 6.5V (typical, channel 1 only)
- Built-in input operational amplifier (channel 1 only)
- Channel 1 input operational amplifier switching function
- Built-in regulator that uses an external PNP transistor and is set by the value of an external resistor.
- Built-in overheat protection (Thermal shutdown) circuit (Design guarantee)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}S$	*1	14	V
	$V_{CC}P$*	$V_{CC}P1$, $V_{CC}P2$ *1	14	V
Maximum input voltage	$V_{IN}B$		13	V
Maximum output current	I_O max	Each output	1	A
MUTE pin voltage	V_{MUTE}		13	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Mounted on the specified board *2	1.8	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*1: All of the power supply pins, $V_{CC}S$, $V_{CC}P1$, and $V_{CC}P2$, must be connected to the power supply system externally to the IC.

*2: Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}S = V_{CC}P1 = V_{CC}P2$ = 8 V, VREF = 2.5 V, MUTE = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Overall						
Quiescent current 1	I_{CC}-ON	All channel outputs on, MUTE pin: high		30	45	mA
Quiescent current 2	I_{CC}-OFF	All channel outputs off, MUTE pin: low		5	10	mA
Muting function on voltage	V_{MUTE}-ON	MUTE ∗1	2			V
Muting function off voltage	V_{MUTE}-OFF	MUTE ∗1			0.5	V
Thermal shutdown	TSD	*4	150	175	200	°C
BTL Amplifier (Channel 1) (Output Amplifier Block)						
Input amplifier offset voltage	V_{OFF}_OP-AMP	Channel 1, input operational amplifiers A and B	-50		+50	mV
Output voltage	V_O1	R_L = 8Ω ∗2	6.2	6.5		V
I/O gain	VG1	∗3	5.4	6	6.6	Times
Slew rate	SR1	With the amplifier operating independently, twice the value measured between outputs ∗3,∗4		0.5		V/μs
Input Operational Amplifier						
Output offset voltage	V_{OFF}1	Input operational amplifiers A and B	-10		+10	mV
OP-AMP_SINK	OP_SINK	Input operational amplifier sink current	2			mA
OP-AMP_SOURCE	OP_SOURCE	Input operational amplifier source current	300	500		μA
Input Operational Amplifier Switching						
Input amplifier switching voltage 1	V_{IN}1-SW	Channel 1, with input operational amplifier B selected ∗5			0.5	V
Input amplifier switching voltage 2	V_{IN}1-SW	Channel 1, with input operational amplifier A selected ∗5	2			V
BTL Amplifier (Channels 2 to 4) (Output Amplifier Block)						
Output offset voltage	V_{OFF}2	Between the + and - outputs for each channel	-50		+50	mV
Output voltage	V_O2	R_L = 8Ω, between the + and - outputs for each channel ∗2	5	5.4		V
I/O gain	VG2		5.4	6	6.6	Multiplier
Slew rate	SR2	Amplifier independently, twice the value measured between outputs ∗3,∗4		0.5		V/μs
Regulator Voltage						
VREG output voltage	VREG	∗6	1.21	1.26	1.31	V
REG-IN sink current	REG-IN-SINK	The base current of the external PNP transistor	5	10		mA
Line regulation	ΔV_OLN	6V ≤ V_{CC} ≤ 12V, I_O = 200mA		20	150	mV
Load regulation	ΔV_OLD	5mA ≤ I_O ≤ 200mA		50	200	mV

*1: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off. (In the amplifier output off state, the outputs are in the high-impedance state.) This operation applies to all channels.

*2: The voltage across the load terminals when an 8Ω load is connected across the outputs. With the input either high or low. With the output in the saturated state.

*3: The channel 1 input operational amplifier has a 0dB gain, i.e. it is a buffer amplifier.

*4: Design guarantee value

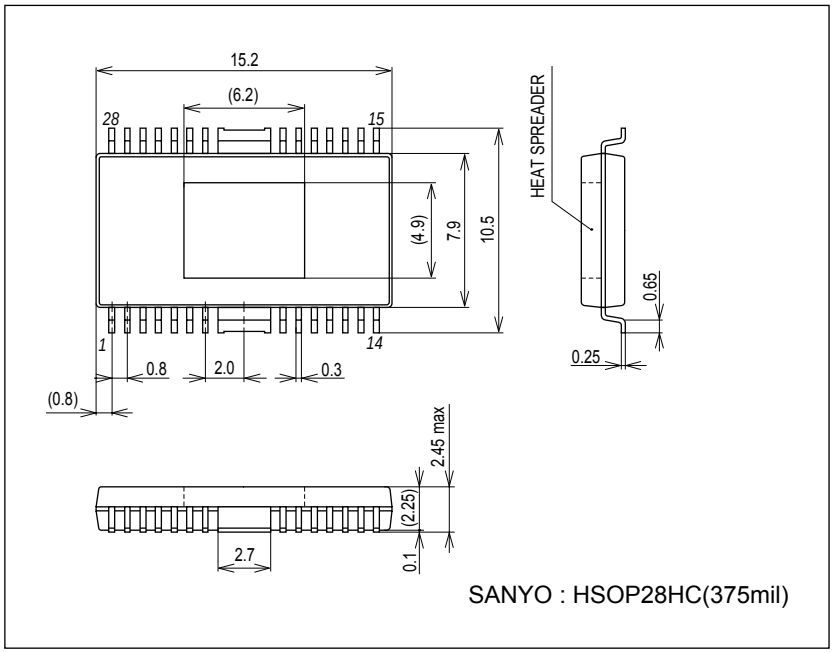
*5: When V_{IN}1-SW is high, operational amplifier A operates, and when low, operational amplifier B operates.

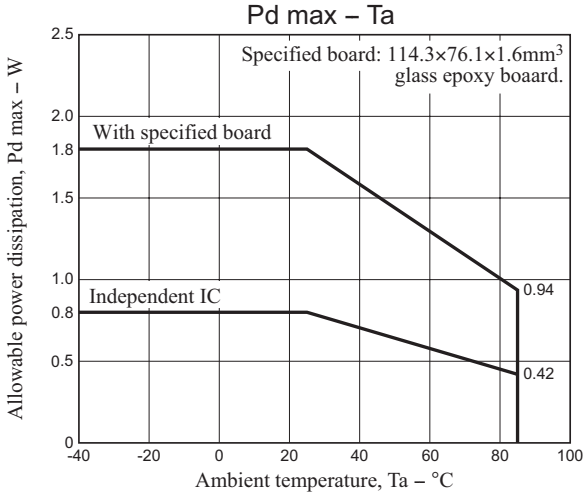
*6: For testing, short the REGOUT to the collector of the external PNP-transistor.

Package Dimensions

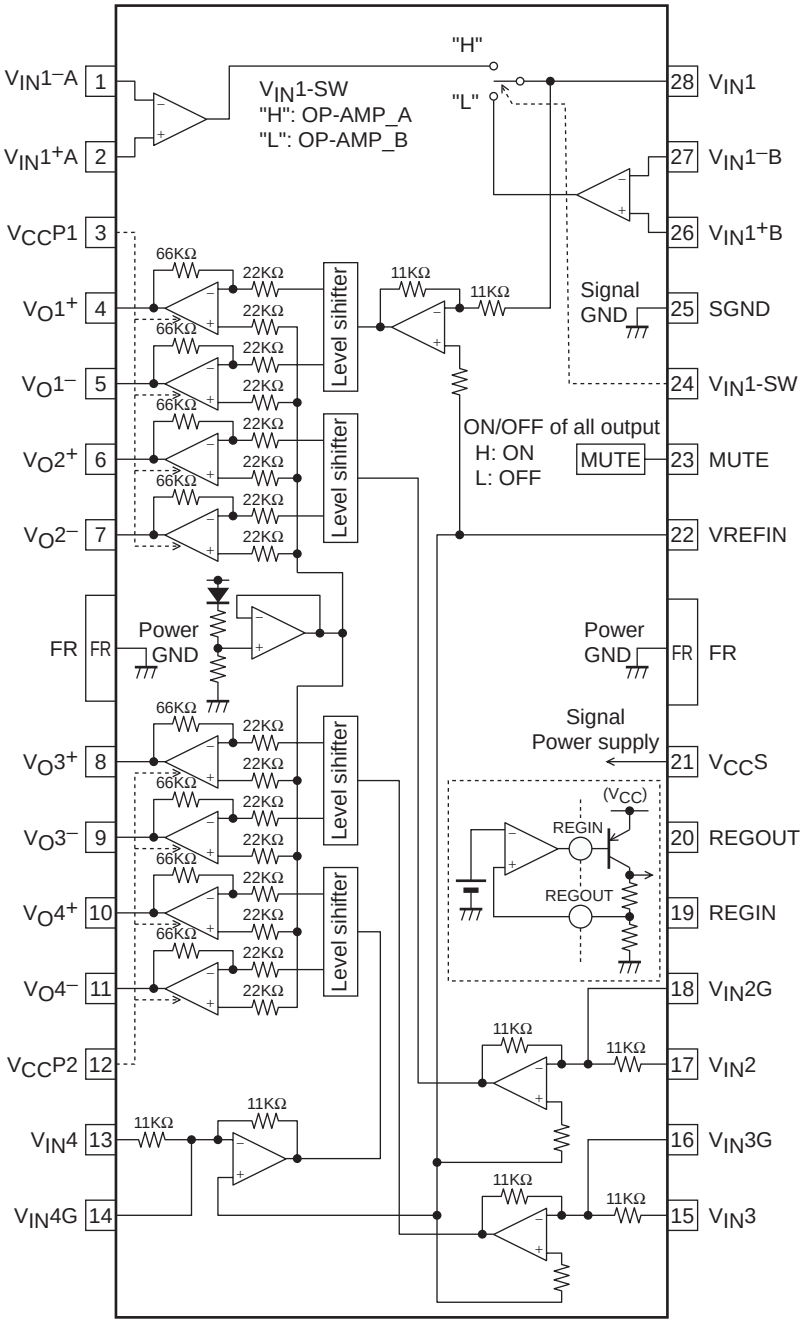
unit : mm (typ)

3234B





Block Diagram



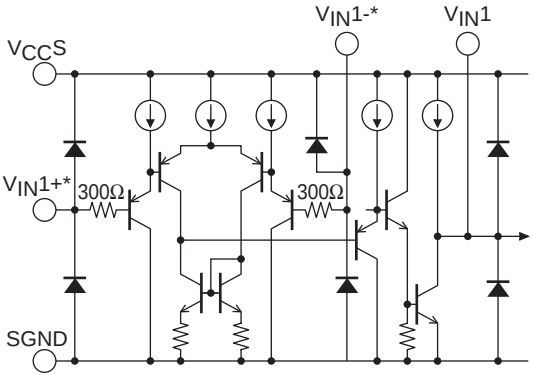
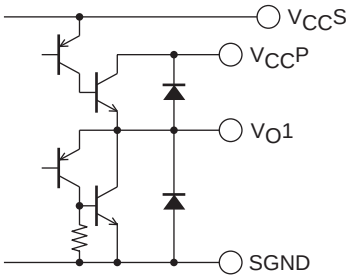
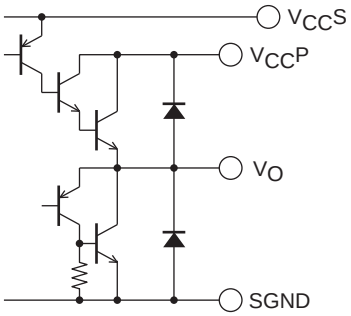
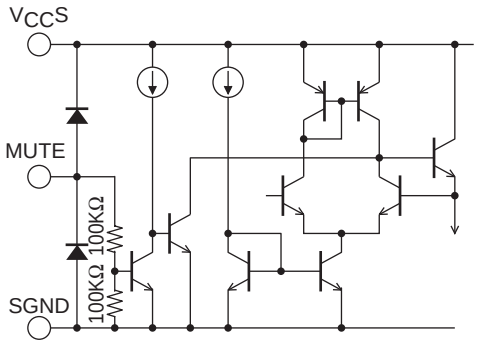
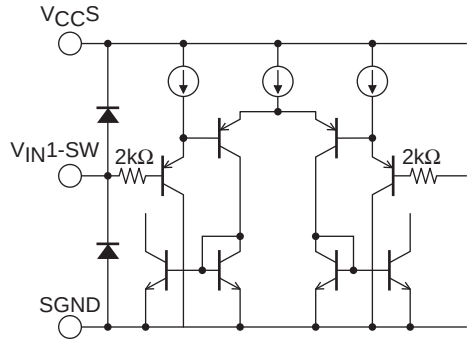
Pin Functions

Pin No.	Pin name	Pin description
1	$V_{IN}1^{-}A$	Channel 1 input amplifier A inverting input
2	$V_{IN}1^{+}A$	Channel 1 input amplifier A non-inverting input
3	$V_{CC}P1$	Channels 1 and 2: power stage power supply
4	V_O1^{+}	Channel 1 output (+)
5	V_O1^{-}	Channel 1 output (–)
6	V_O2^{+}	Channel 2 output (+)
7	V_O2^{-}	Channel 2 output (–)
8	V_O3^{+}	Channel 3 output (+)
9	V_O3^{-}	Channel 3 output (–)
10	V_O4^{+}	Channel 4 output (+)
11	V_O4^{-}	Channel 4 output (–)
12	$V_{CC}P2$	Channels 3 and 4: power stage power supply
13	$V_{IN}4$	Channel 4 input
14	$V_{IN}4G$	Channel 4 input (gain adjustment)
15	$V_{IN}3$	Channel 3 input
16	$V_{IN}3G$	Channel 3 input (gain adjustment)
17	$V_{IN}2$	Channel 2 input
18	$V_{IN}2G$	Channel 2 input (gain adjustment)
19	REGIN	Base connection of external PNP transistor
20	REGOUT	Regulator error amplifier input (+)
21	$V_{CC}S$	Signal system power supply
22	VREFIN	Reference voltage input
23	MUTE	Output on/off control
24	$V_{IN}1$-SW	Channel 1 input operational amplifier switching
25	SGND	Signal system ground
26	$V_{IN}1^{+}B$	Channel 1 amplifier B non-inverting input
27	$V_{IN}1^{-}B$	Channel 1 amplifier B inverting input
28	$V_{IN}1$	Channel 1 input and input operational amplifier output

Note: • The center frame (FR) is used as the power system ground (P-GND). Along with the signal system ground (SGND), this level must be the lowest potential in the system.

• The $V_{CC}S$ (signal system power supply), $V_{CC}P1$, and $V_{CC}P2$ (output stage power supplies) must be shorted together externally.

Pin Description

Pin No.	Pin name	Function	Description	Equivalent circuit
1 2 26 27 28	$V_{IN}1^{-}A$ $V_{IN}1^{+}A$ $V_{IN}1^{+}B$ $V_{IN}1^{-}B$ $V_{IN}1$	Input (channel 1)	Inputs The total gain is set by setting the gain of the input amplifier.	
4 5	V_O1^{+} V_O1^{-}	Output (channel 1)	Channel 1 output	
6 7 8 9 10 11	V_O2^{+} V_O2^{-} V_O3^{+} V_O3^{-} V_O4^{+} V_O4^{-}	Output (channels 2 to 4)	Channel 2 to 4 outputs	
23	MUTE	MUTE	Controls the on/off states of the corresponding channel output. MUTE = high: Output on MUTE = low: Output off ∗: When the MUTE pin is open, the outputs will be off. (The same as when the MUTE pin is low.)	
24	$V_{IN}1$-SW	Channel 1 input amplifier switching	Channel 1 input operational amplifier switching function. Either amplifier A or amplifier B is selected according to the voltage applied to the VIN1-SW pin. High: V_{IN}_A Low: V_{IN}_B	

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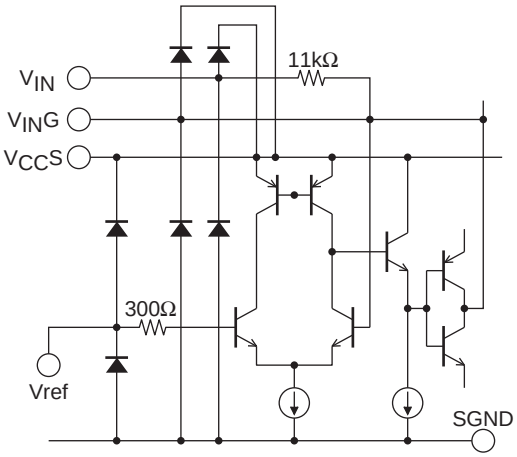
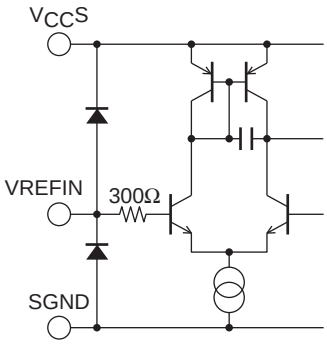
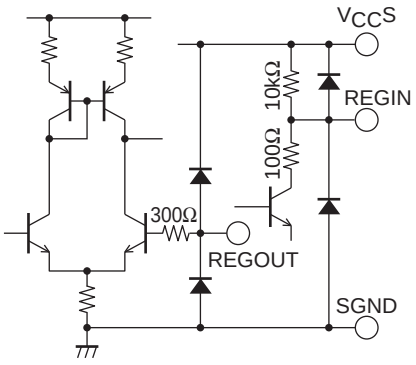
Pin No.	Pin name	Function	Description	Equivalent circuit
17 18 15 16 13 14	$V_{IN}2$ $V_{IN}2G$ $V_{IN}3$ $V_{IN}3G$ $V_{IN}4$ $V_{IN}4G$	Input (channels 2 to 4)	Inputs	
22	VREFIN	VREF	Reference voltage	
19 20	REGIN REGOUT	REG	Regulator block	

MUTE, V_{IN}1-SW

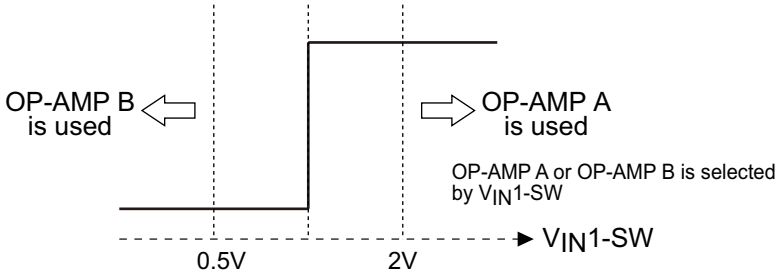
- Relationship between the MUTE pin and the outputs

MUTE	Outputs			
	CH1	CH2	CH3	CH4
H	on			
L	off			

Note ∗1: When the outputs are off, they are in the high-impedance state.
∗2: The muting function applies to all channels.

- V_{IN}1-SW and the channel 1 input operational amplifier

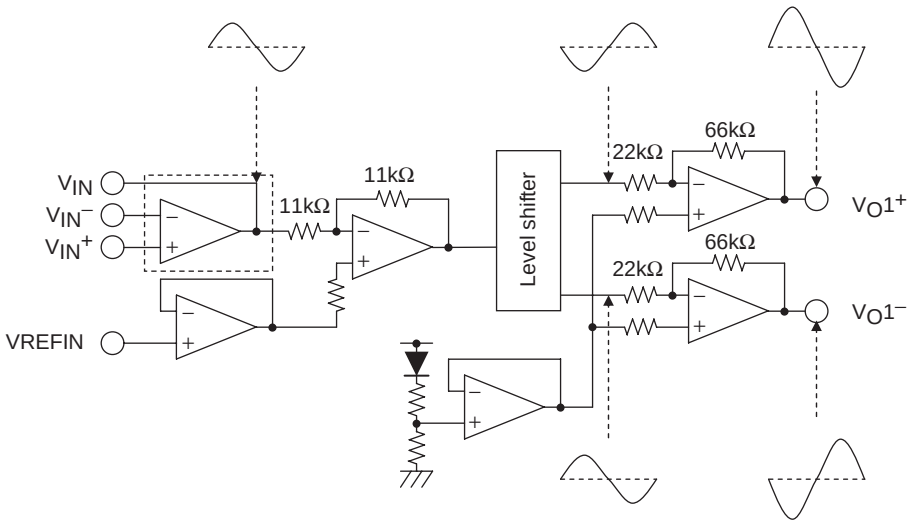
V_{IN}1-SW	Channel 1 input operational amplifier
H	AMP_A
L	AMP_B



- Muting

MUTE	Output amplifiers
L	off
H	on

Overview of the input/output relationship



Note: Only channel 1 has an added input operational amplifier.

Application Circuit Example