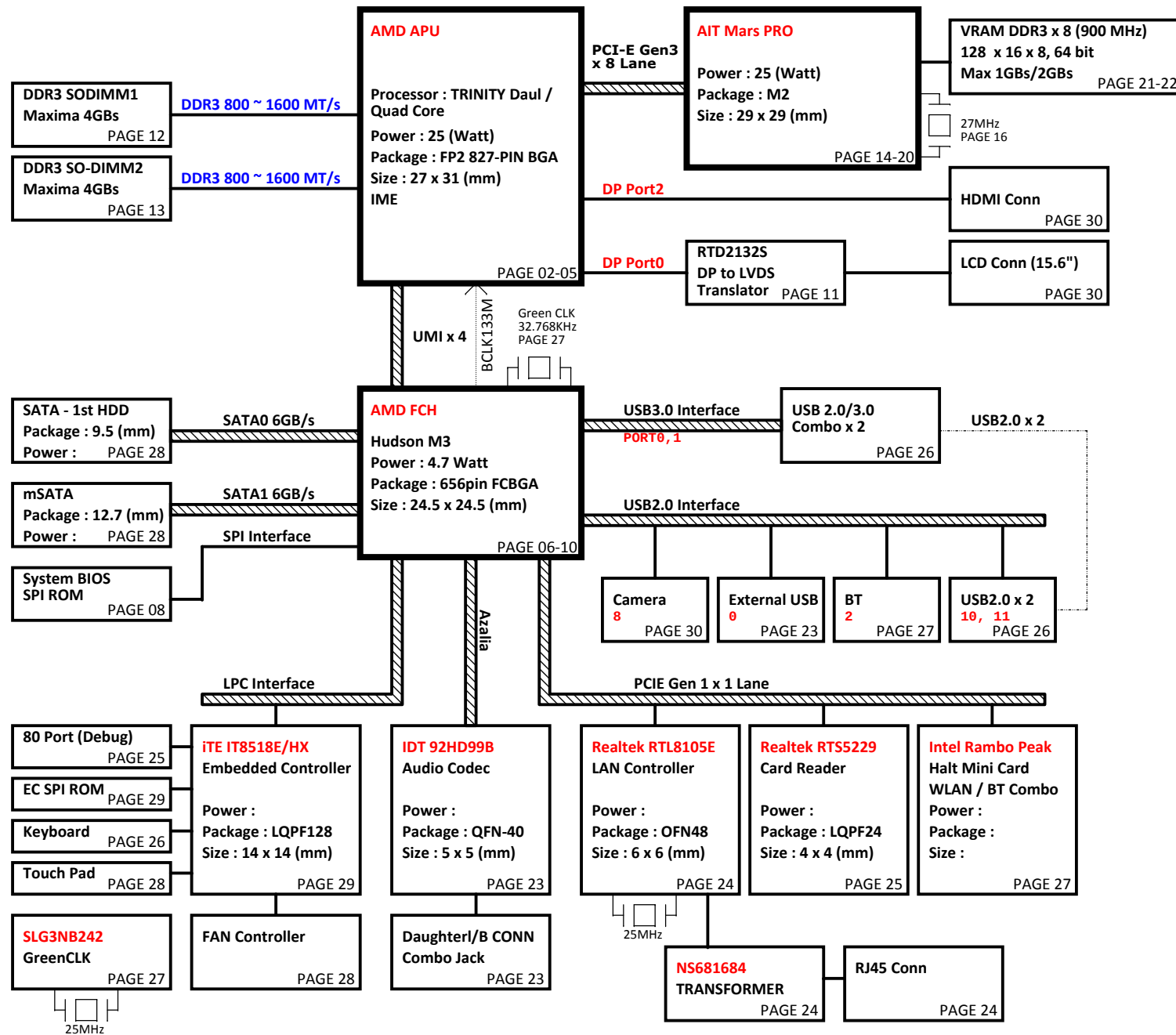


Volks_AMD Comal DIS/UMA (14") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

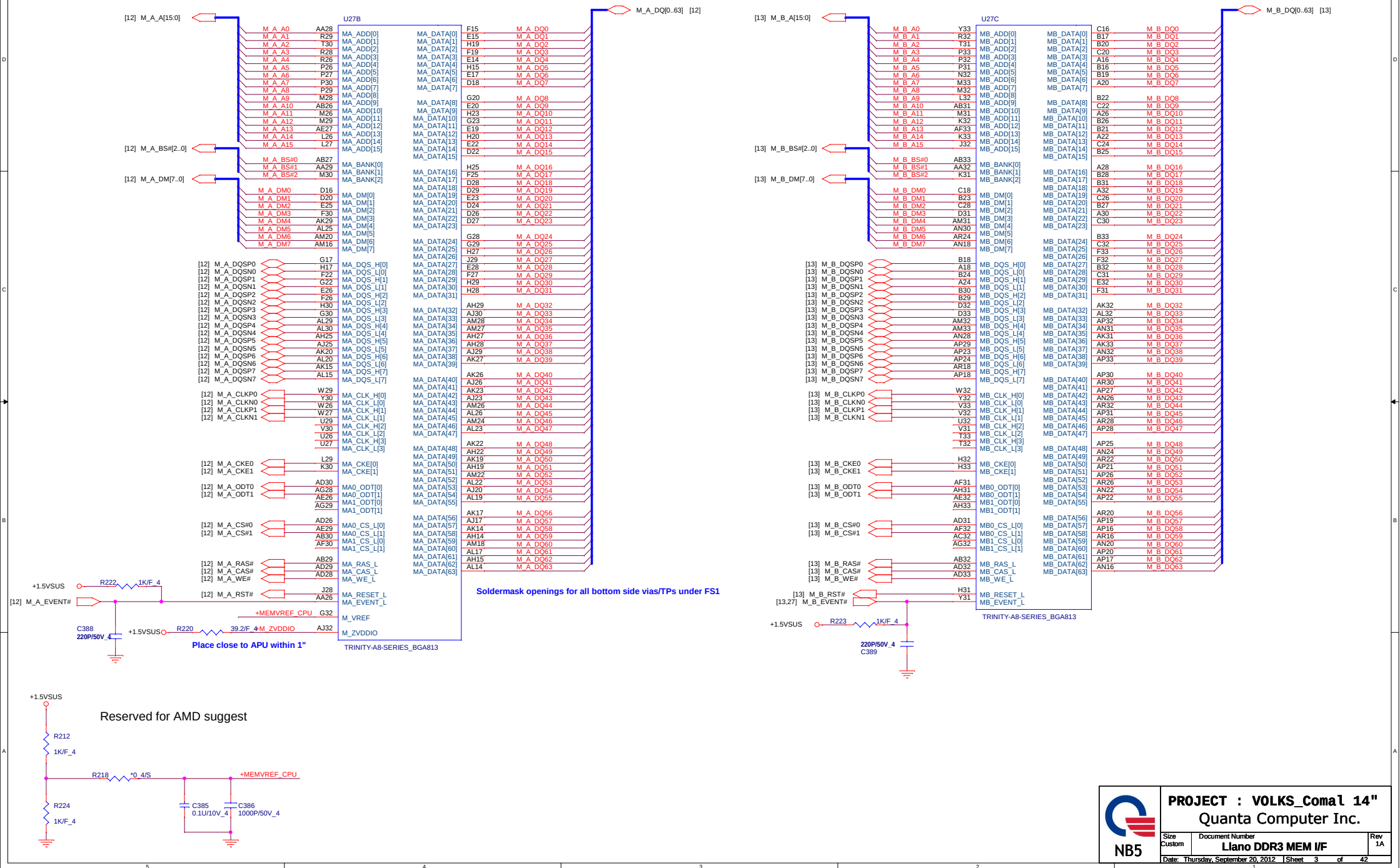
RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



PROJECT : VOLKS_Comal 14"
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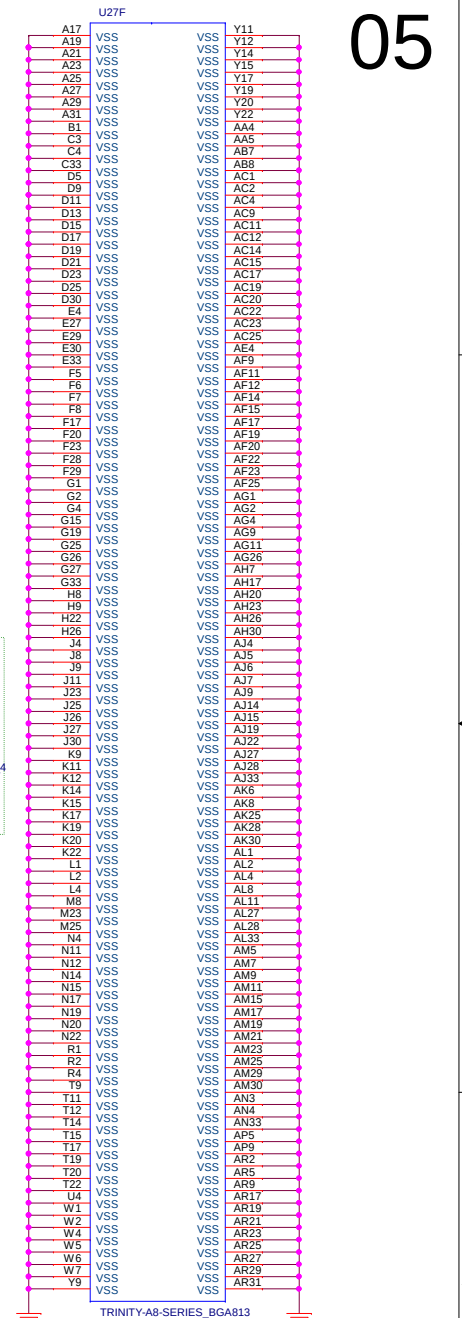
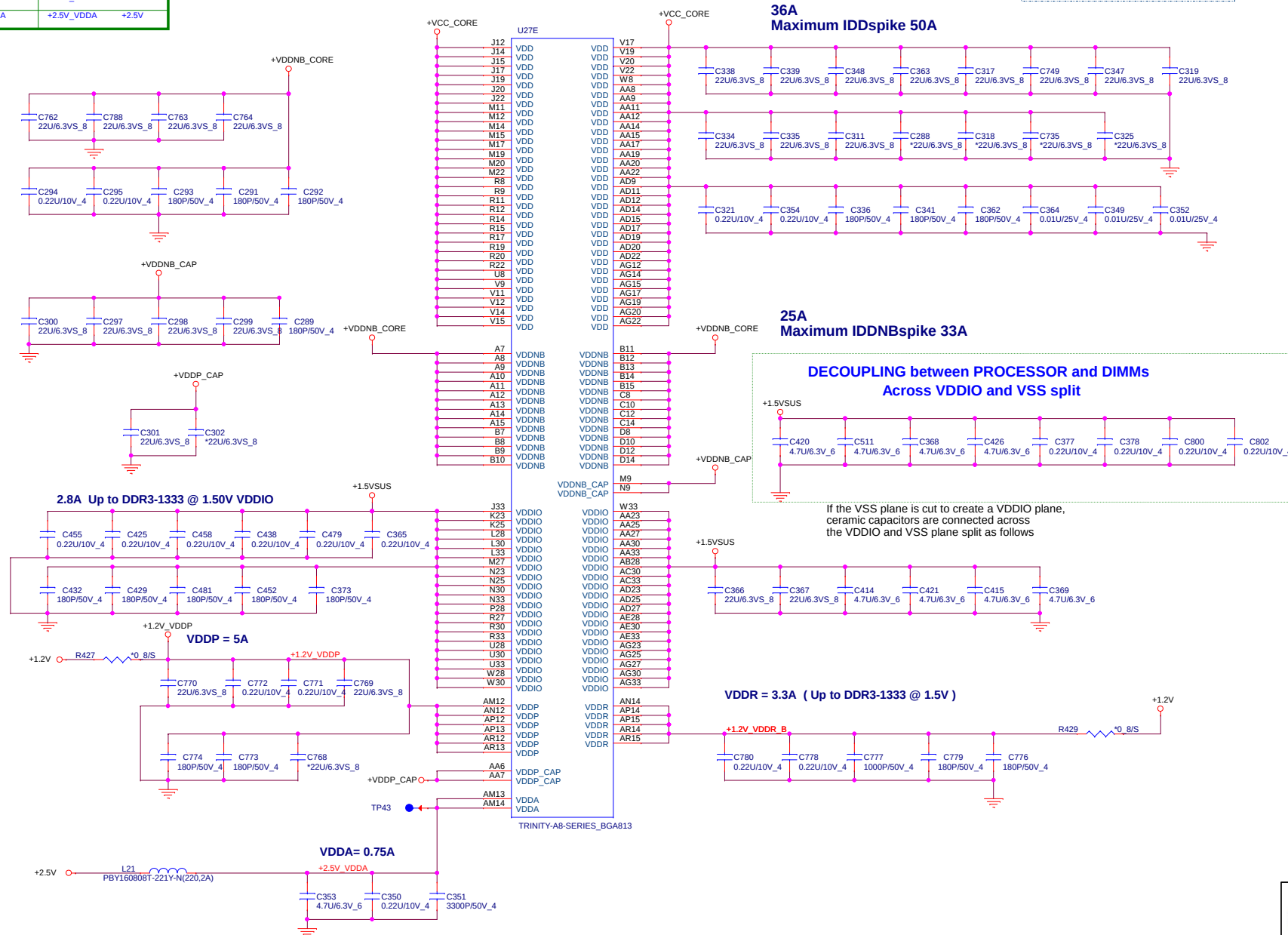
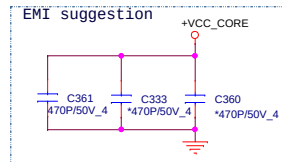
Size A3 Document Number Rev 1A
Block Diagram
Date: Thursday, September 20, 2012 | Sheet 1 of 42





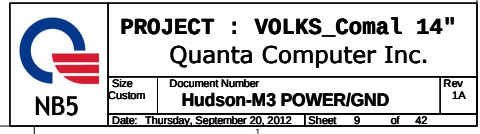
APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



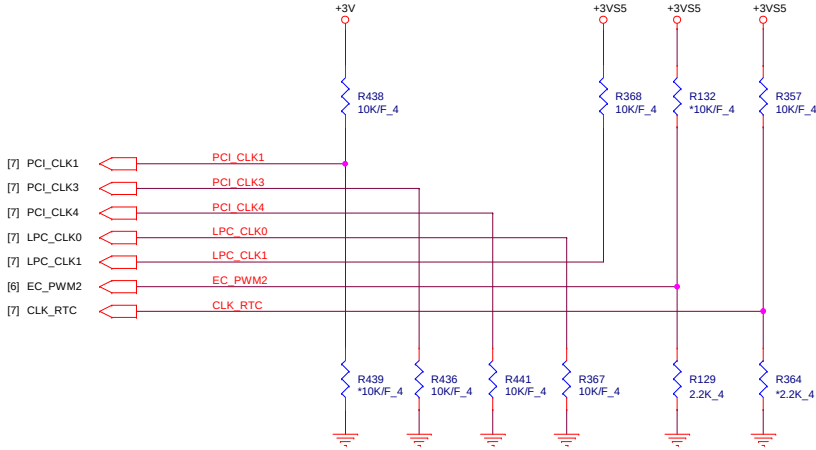






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

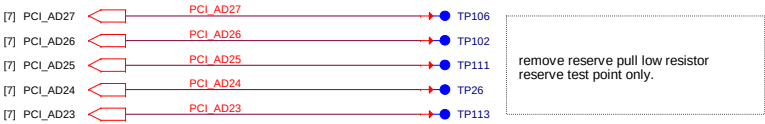


REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

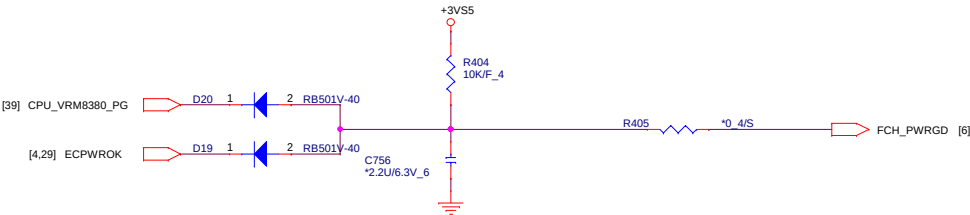
DEBUG STRAPS

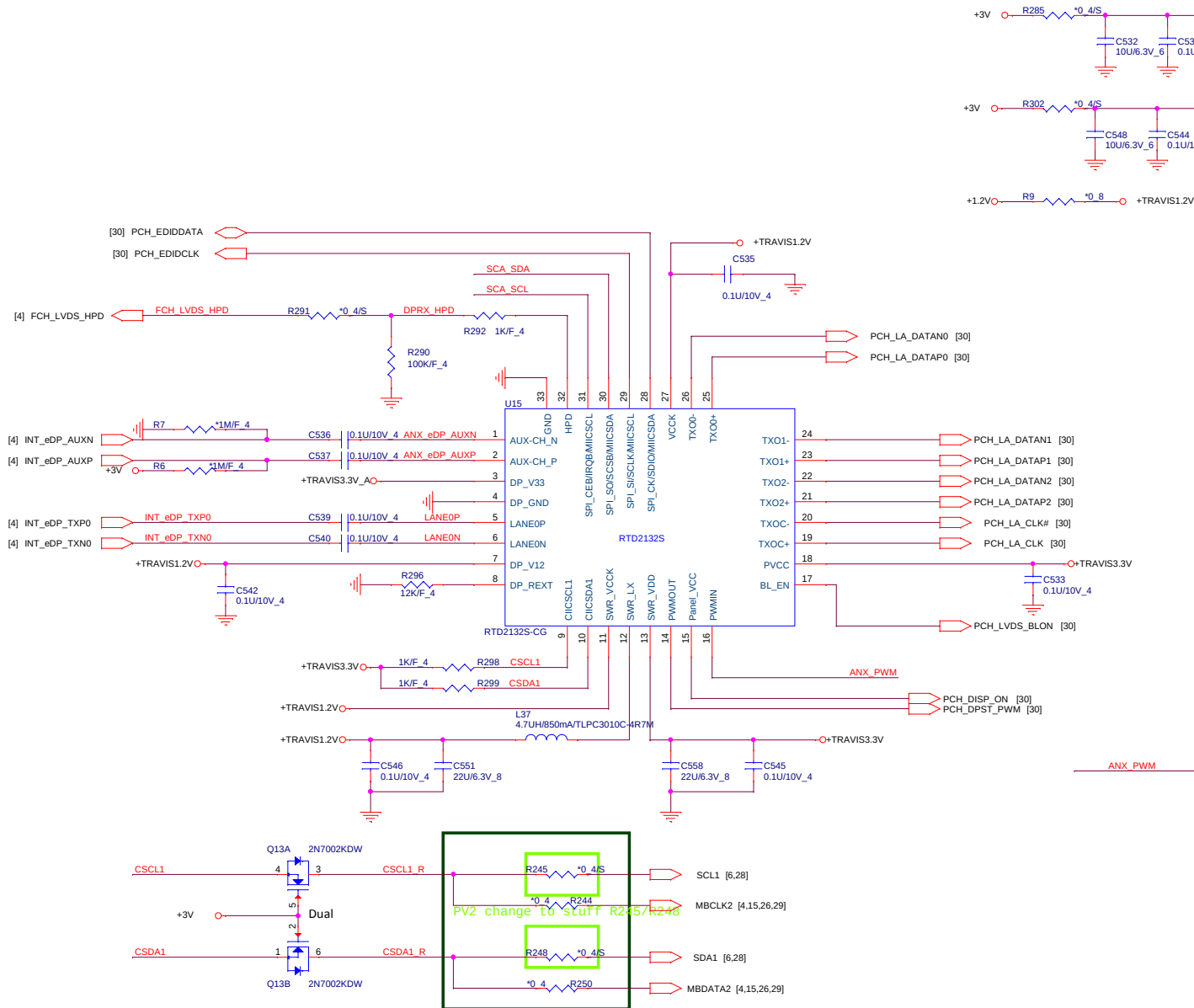
FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

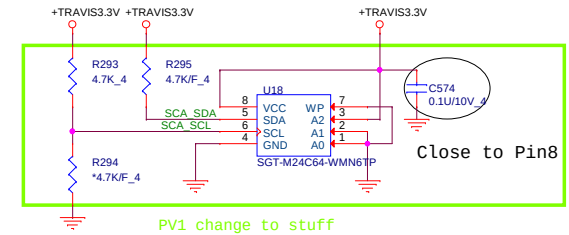
FCH_PWRGD



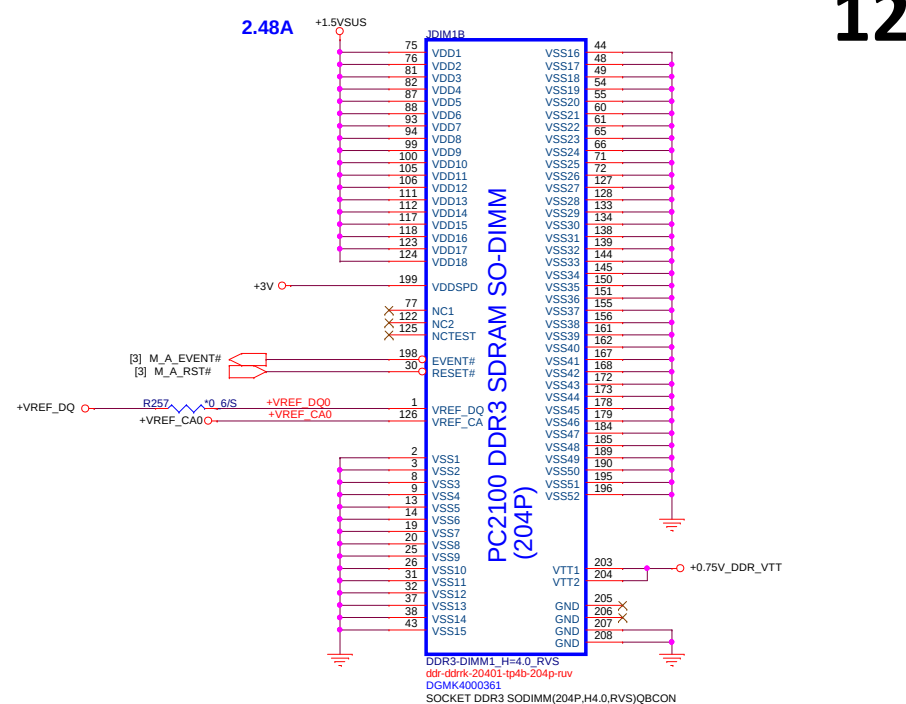
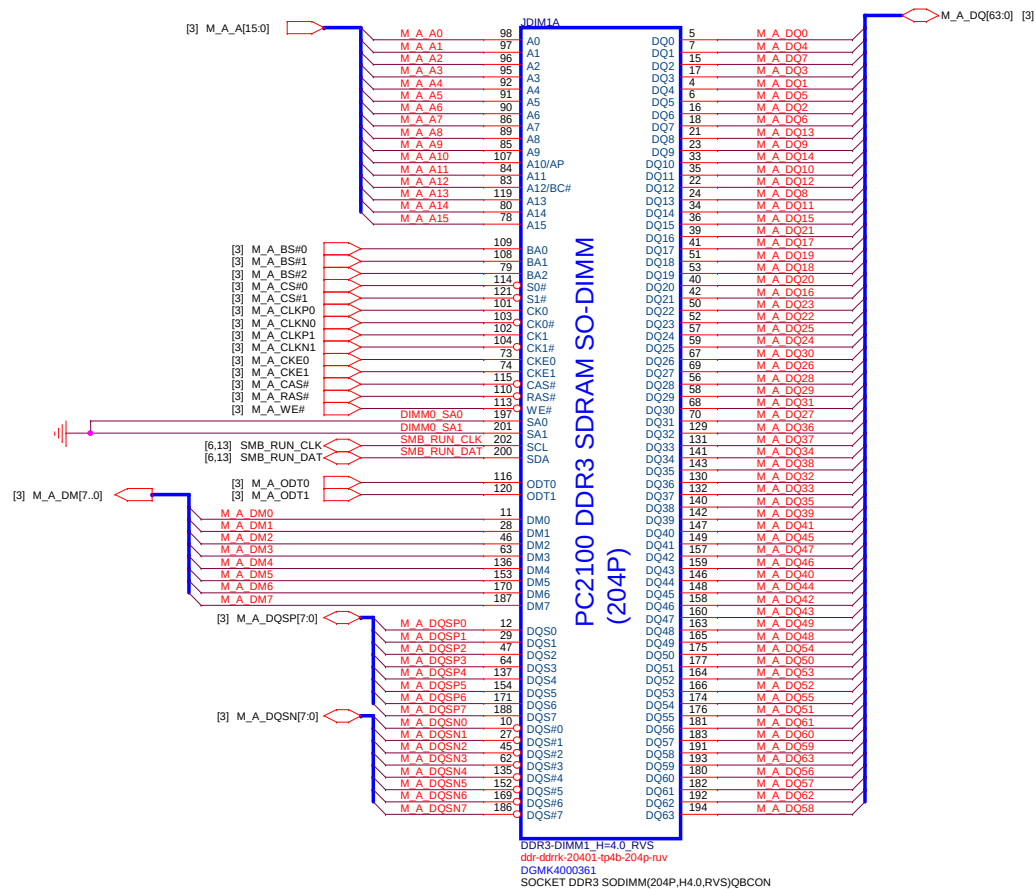


SCA_SCL pull high => EEPROM mode
SCA_SDA pull low => EEPROM Free mode

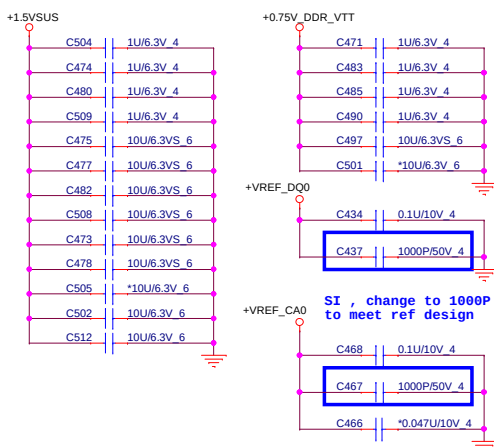
Address=0xA8



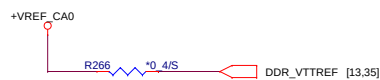
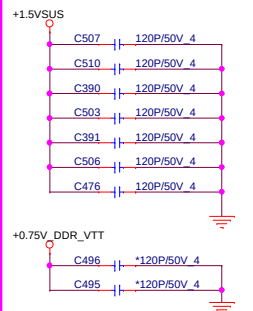
EE PROM R3054, R3056
EC OPTION R3055, R3057



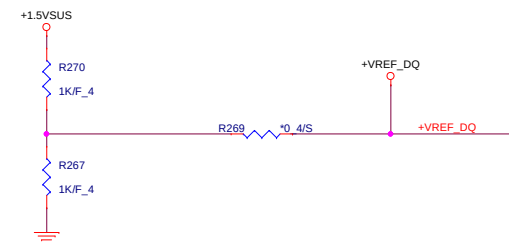
Place these Caps near So-Dimm0.

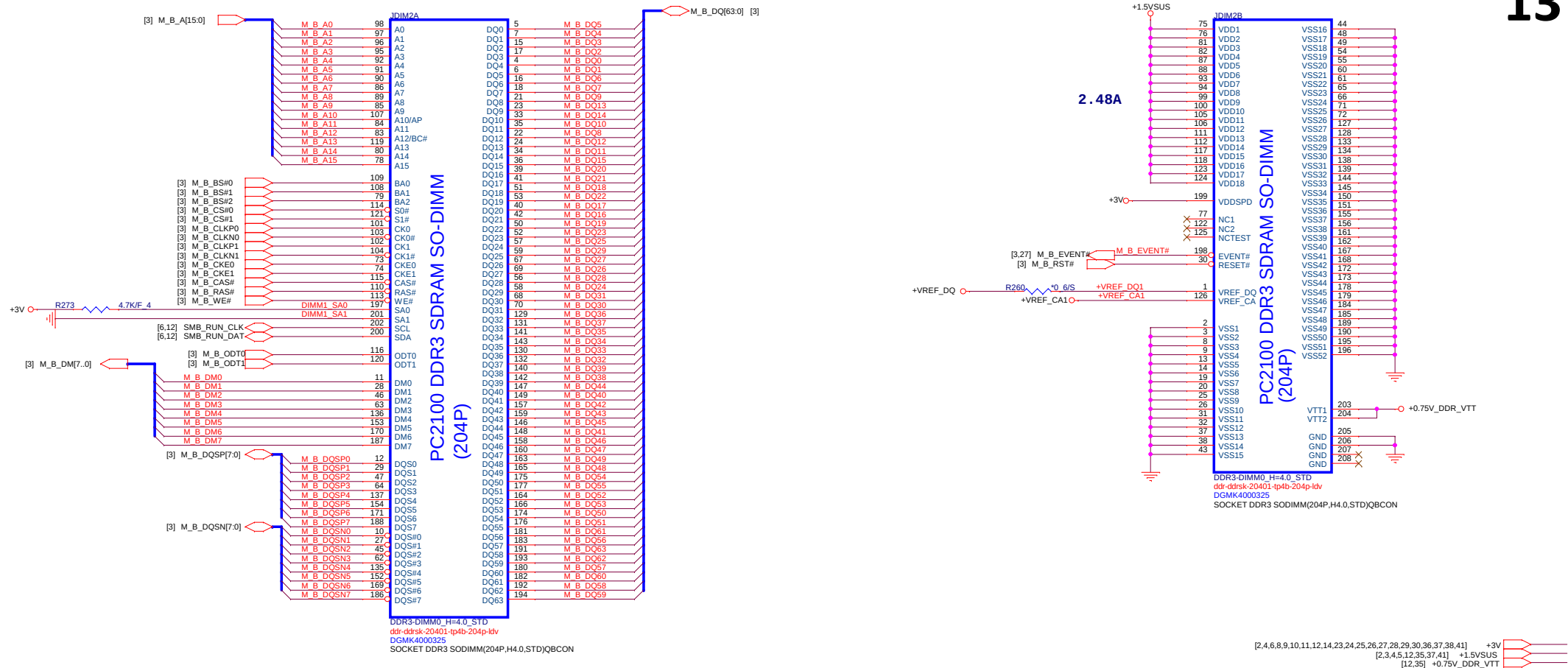


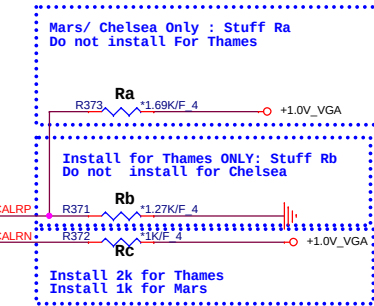
For EMI RESERVE



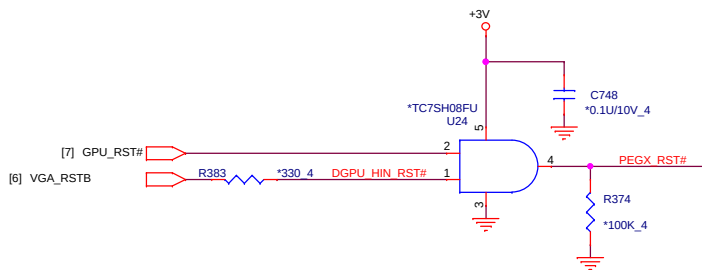
Reserved for AMD suggest



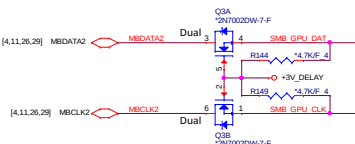
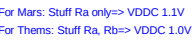




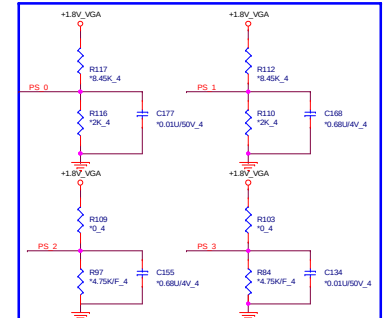
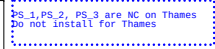
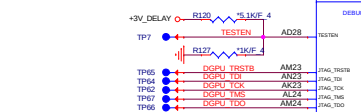
	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



GPI030 GPI012 GPI016 GPI020 GPI015 Thames XT

[illegible]

For Mars: Stuff Ra only=> VDDC 1.1V
For Them: Stuff Ra, Rb=> VDDC 1.0V




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Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_psm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwrss_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_3[0]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

⋮ CX8PG471000/BLM18PG471\$N1D/1A_6

```

: For Thems: La,Lb:

```

⋮ CX8PG471000/BLM18PG471\$N1D/1A_6

U231

PART 9 OF 9

AN32 DPLL_PVDD

AN31 DPLL_VDDC

AN32 DPLL_PVSS

XTALIN AV23 EVGA-XTALI

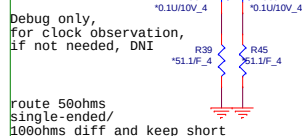
XTALOUT AU34 EVGA-XTALO

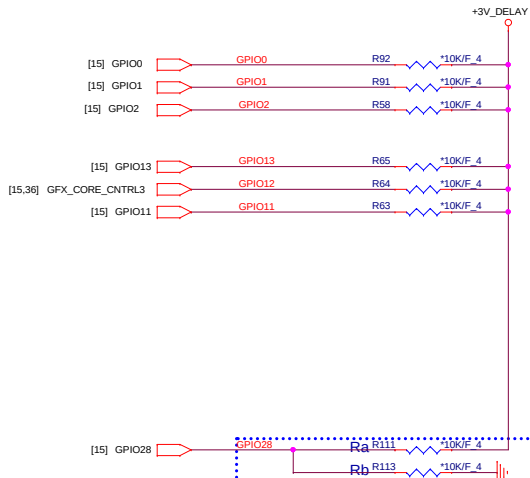
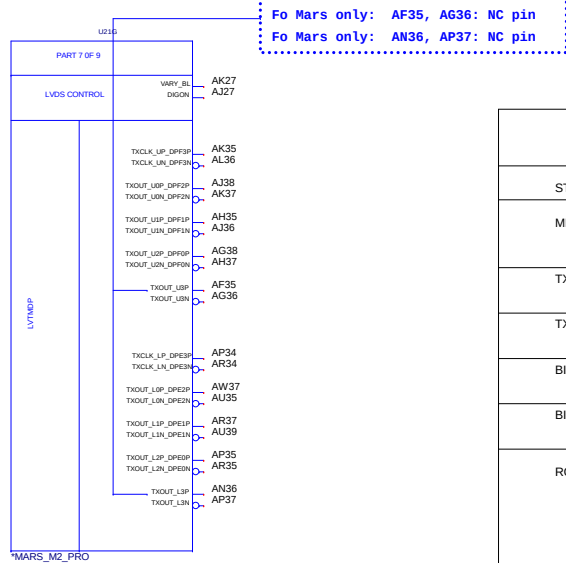
R34 10M

Y2 27MHZ

C52 22PF50V_4

C63 22PF50V_4





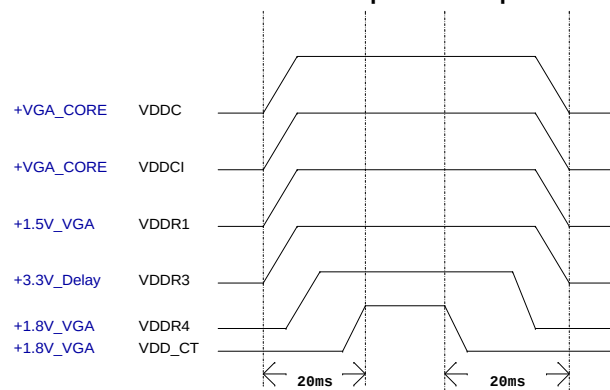
Memory Aperture size:

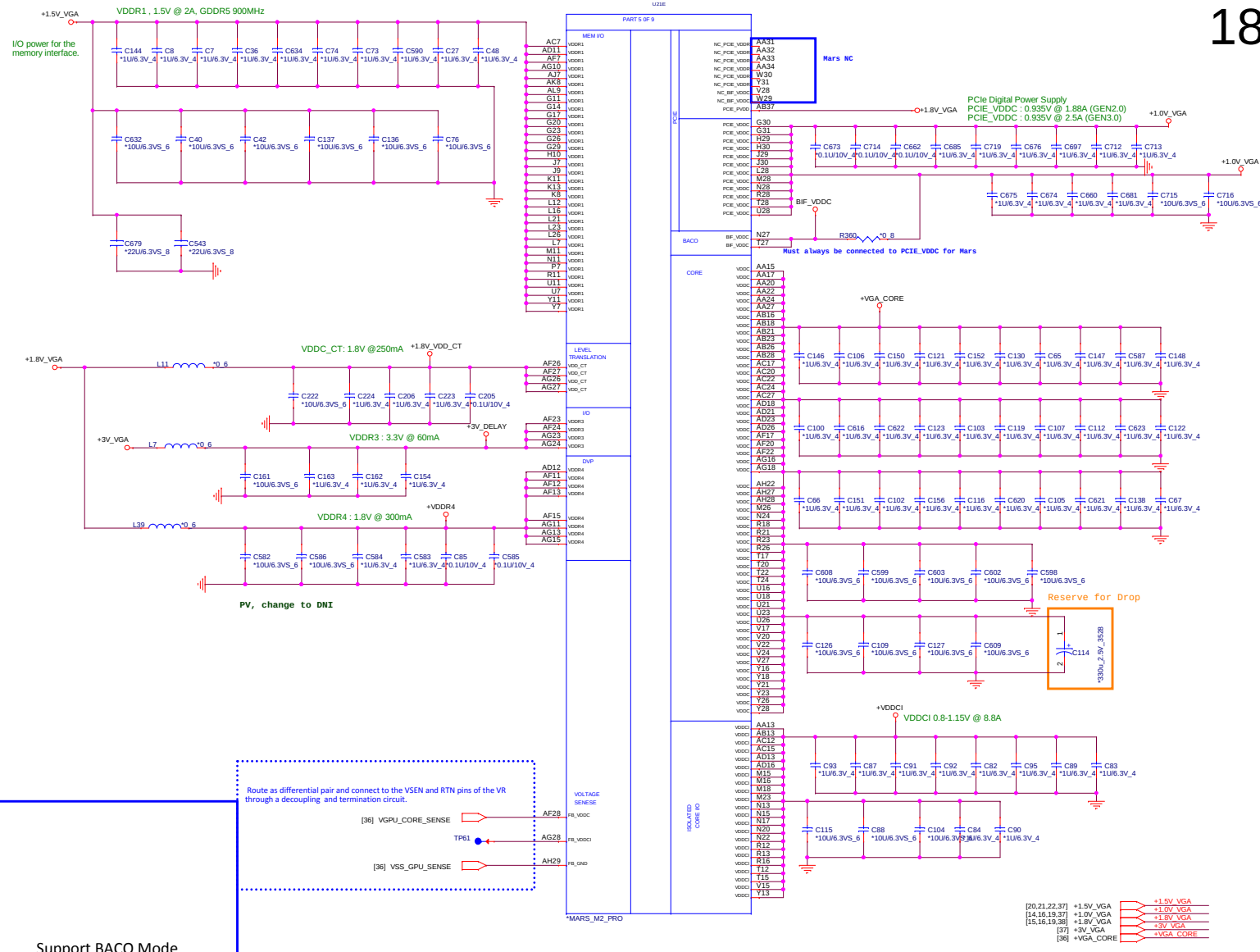
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS -- SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (STD) 101 - 1Mbit M25P10A (STD) 101 - 2Mbit M25P20 (STD) 101 - 4Mbit M25P40 (STD) 101 - 8Mbit M25P80 (ST) 101 - 512Kbit Fm25LV512 (Chingis) 101 - 1Mbit Fm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, it is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Power Up/Down Sequence

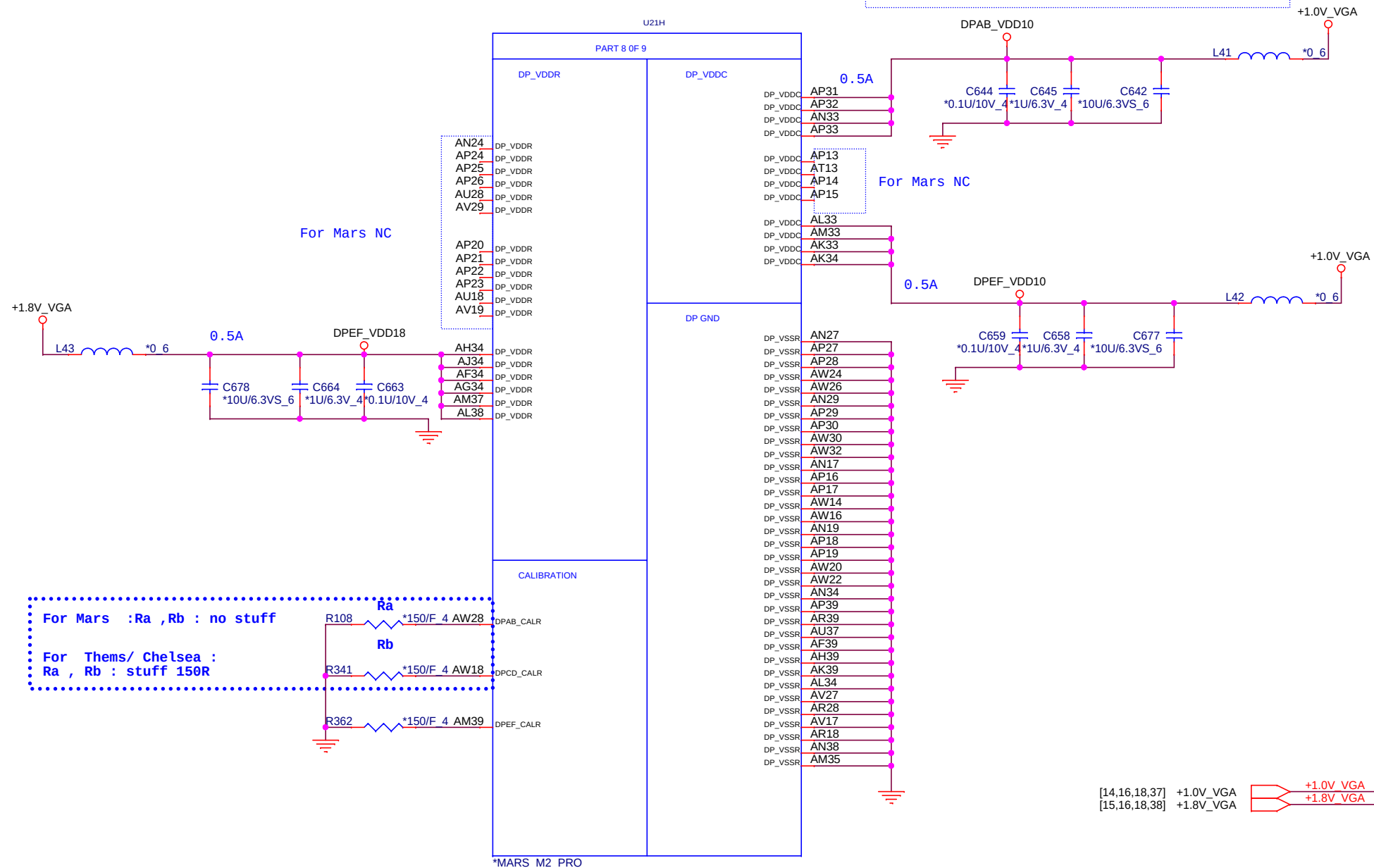


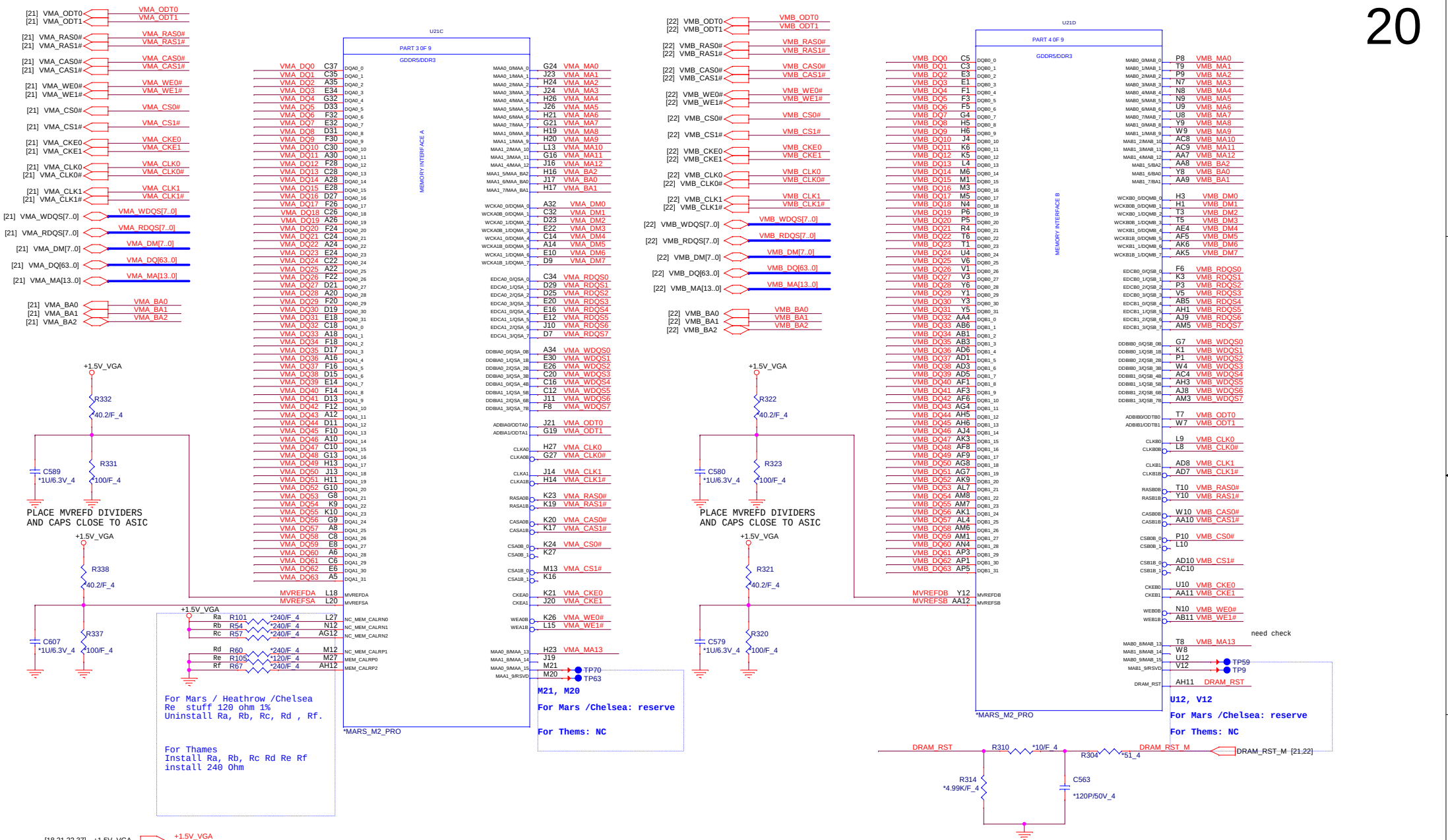


Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

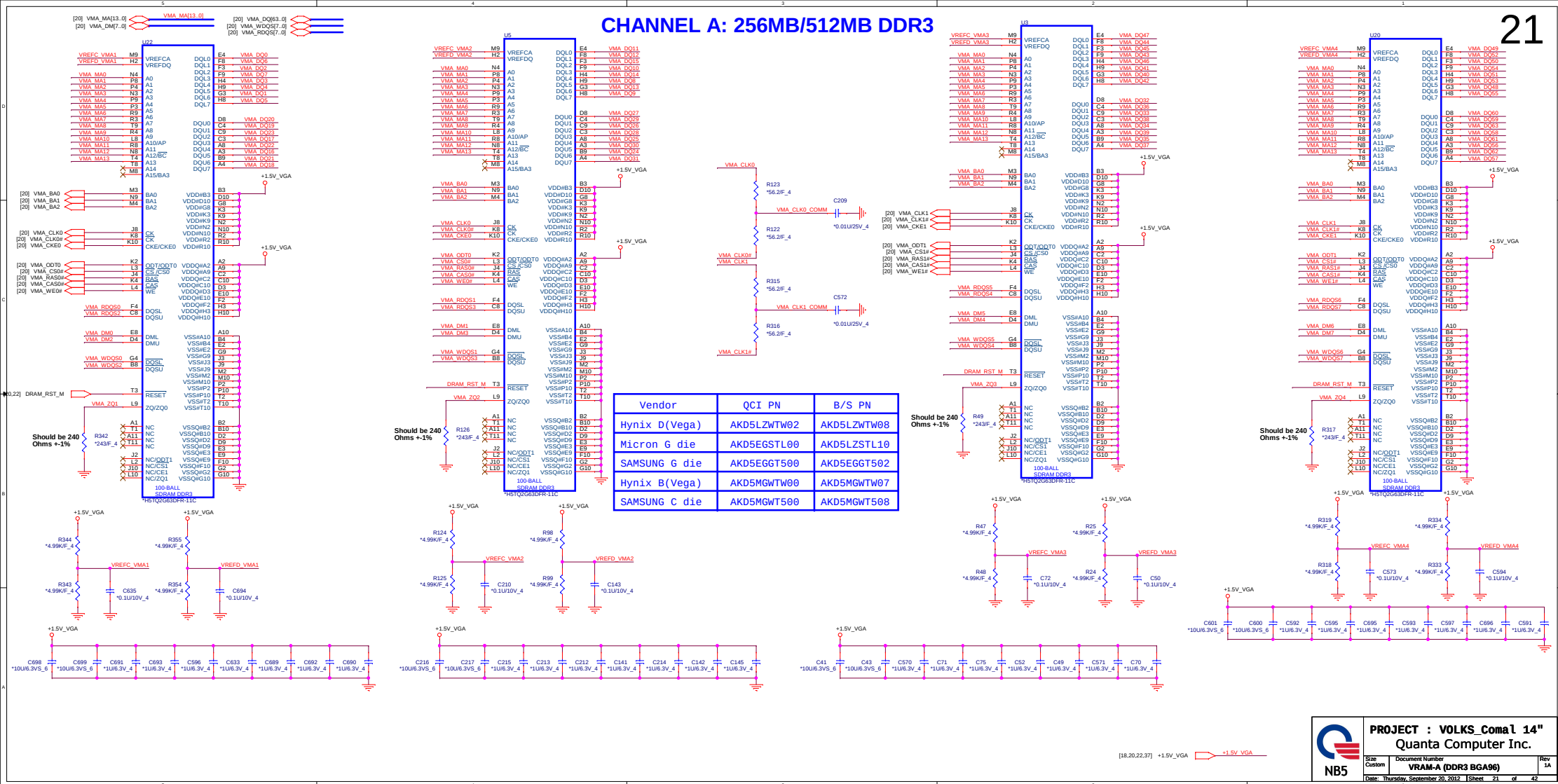
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE





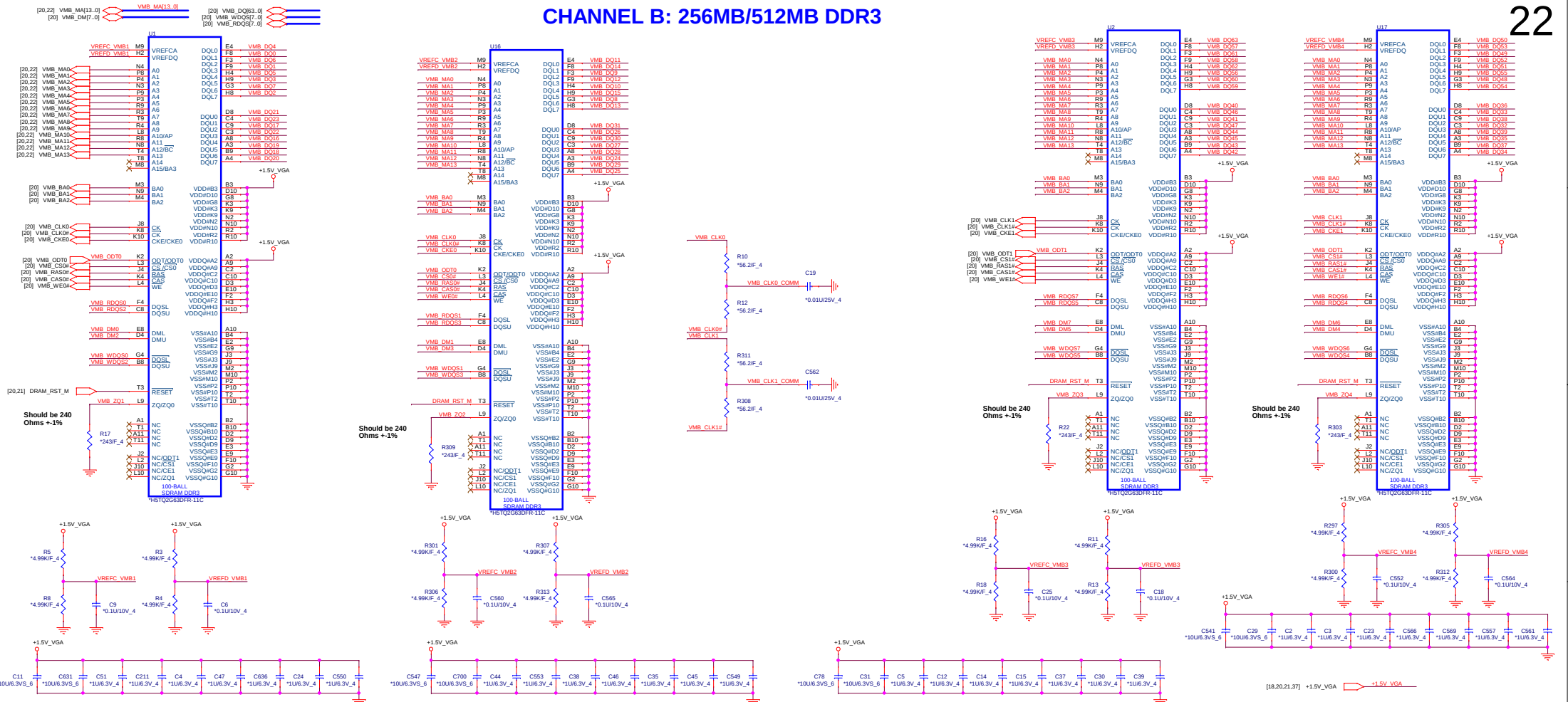
PROJECT : VOLKS_Coma1 14"
Quanta Computer Inc.

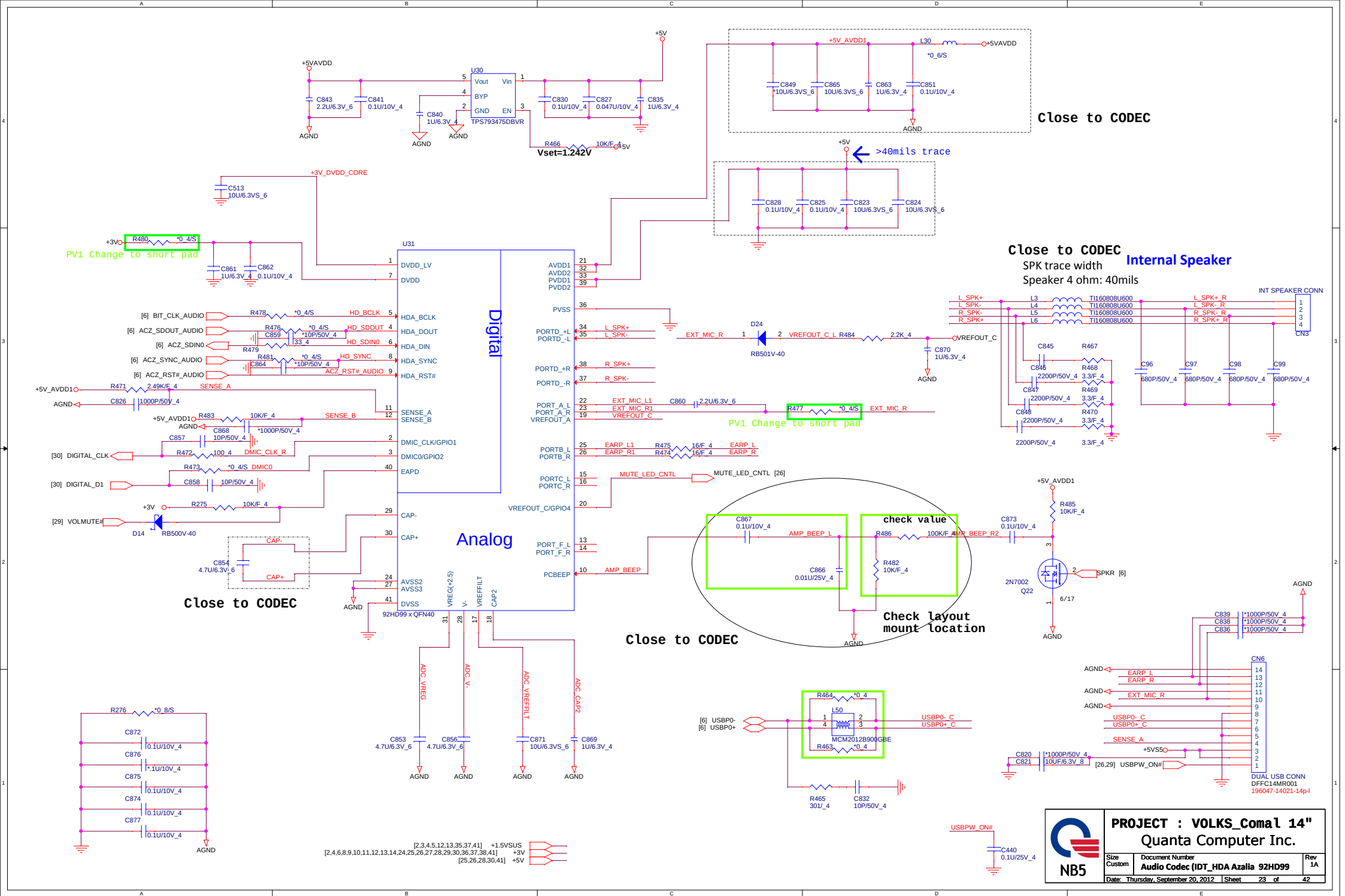
Size Custom	Document Number Mars_MEM_Interface	Rev 1A
Date: Thursday, September 20, 2012		Sheet 20 of 42

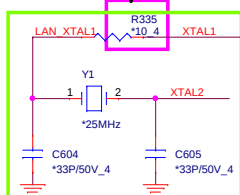


CHANNEL B: 256MB/512MB DDR3

22





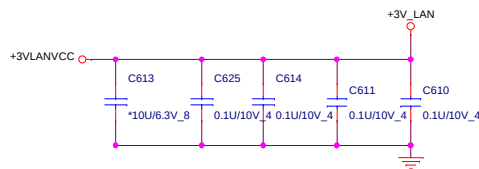
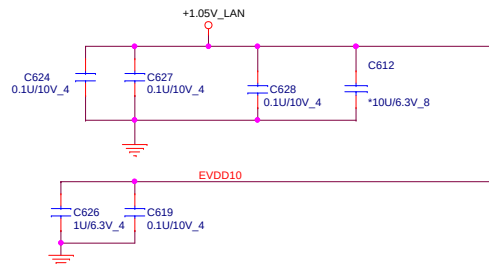
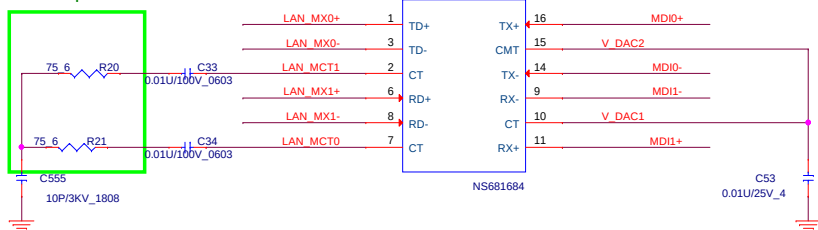
For EMI $\theta \sim 22 \text{ ohm}$ 

PV2 change to non-stuff for Green Clock solution

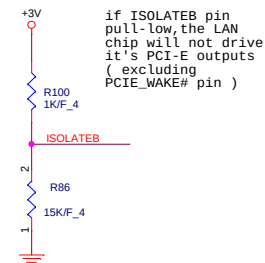
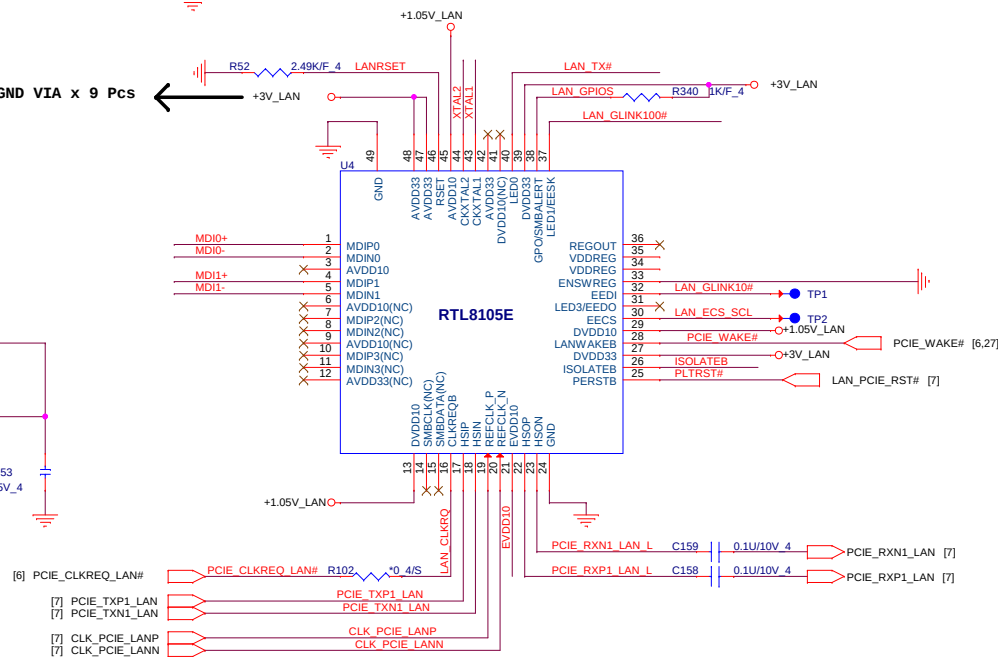
Green Clk

[27] LAN_XTAL25_IN $\rightarrow$ R336 510/F_4 XTAL2
PV2 change to stuff for Green Clock solution

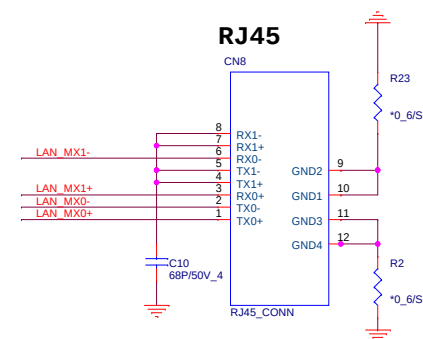
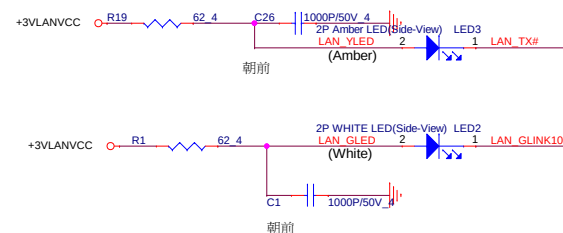
Change to 0603 size for EMI request



GND VIA x 9 Pcs

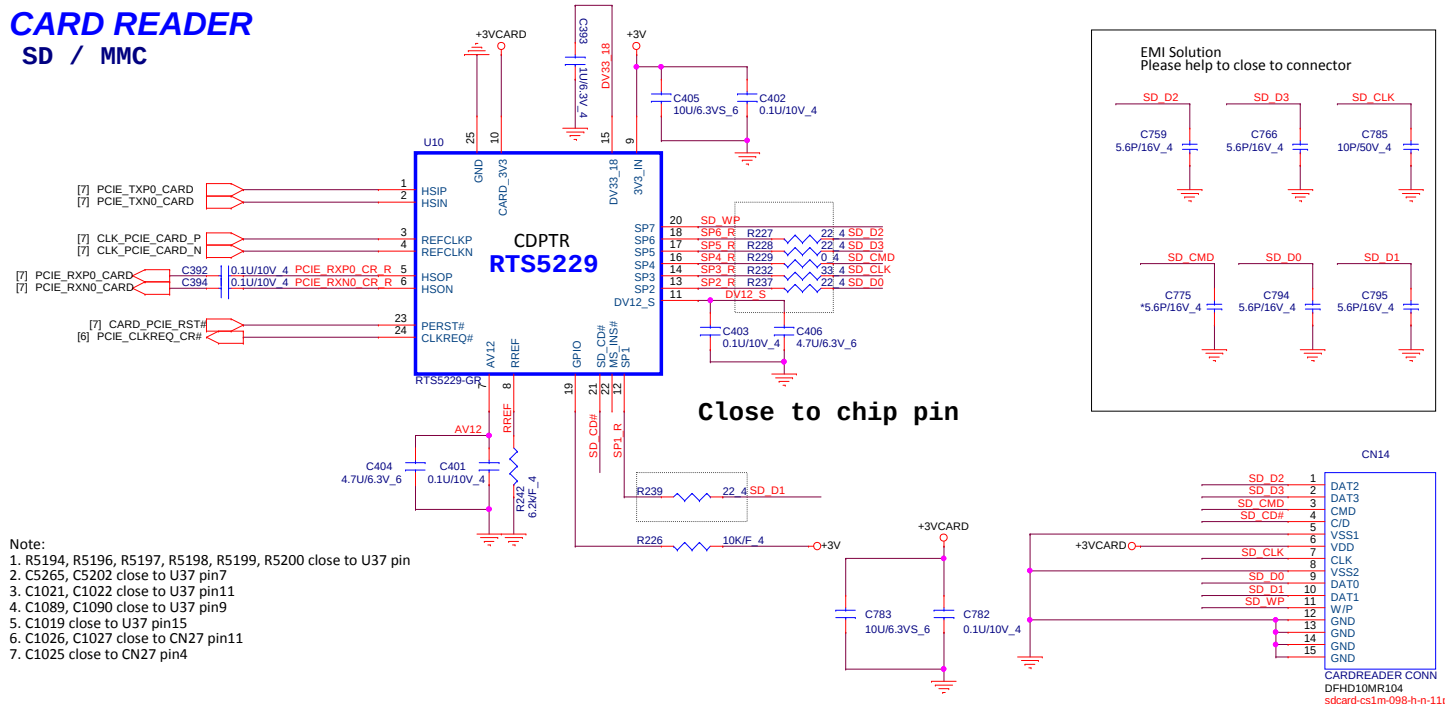


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

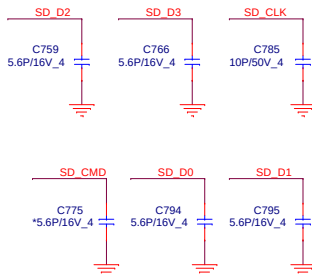


CARD READER

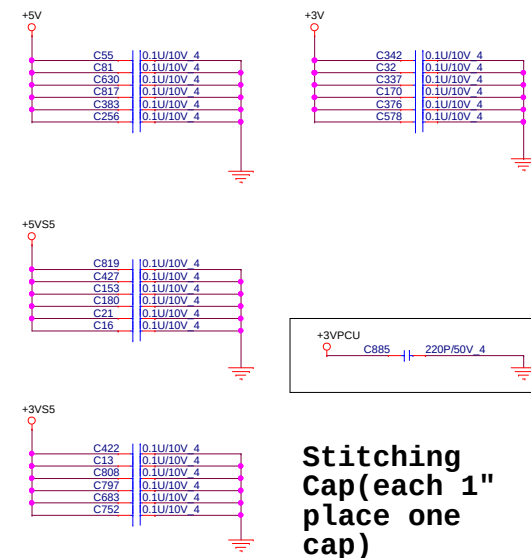
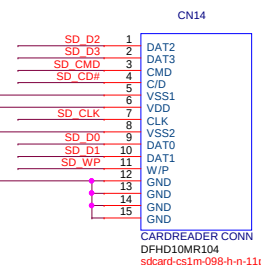
SD / MMC



EMI Solution
Please help to close to connector

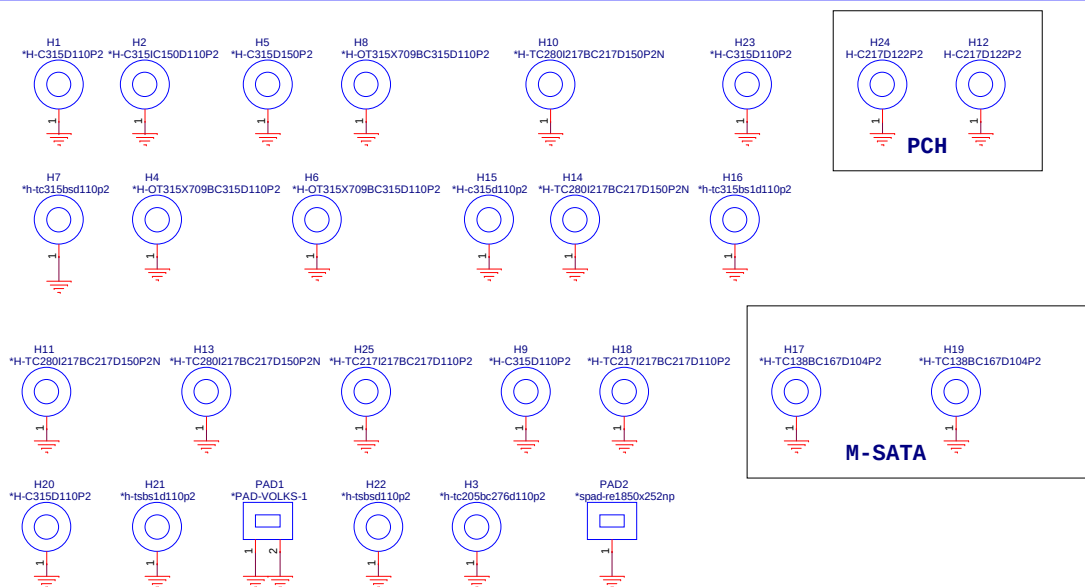


Close to chip pin

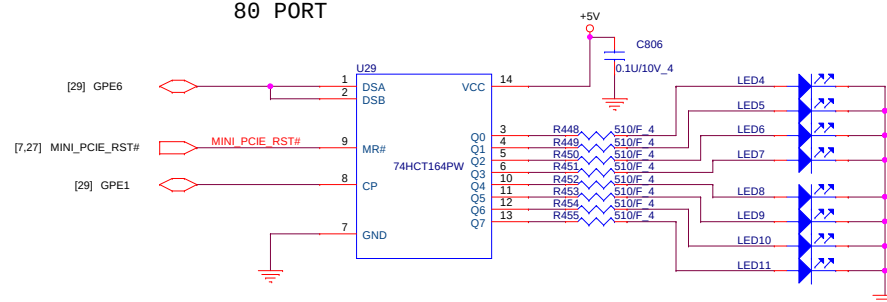


Stitching
Cap(each 1"
place one
cap)

EMI/ESD

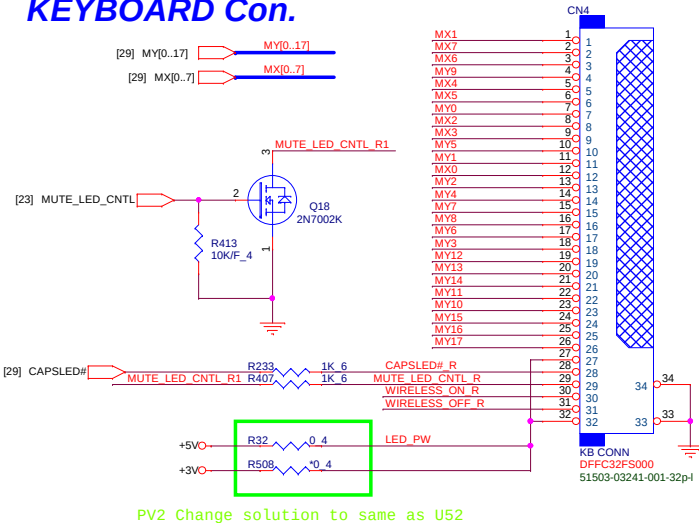


80 PORT



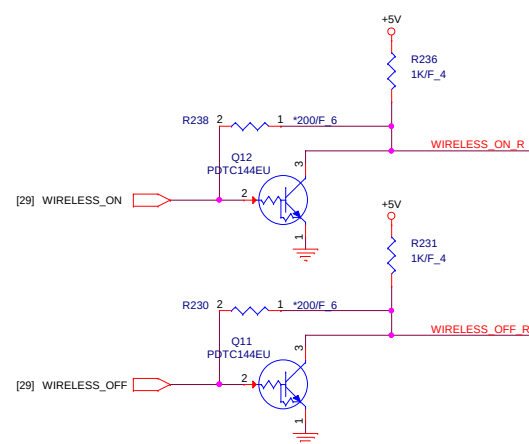
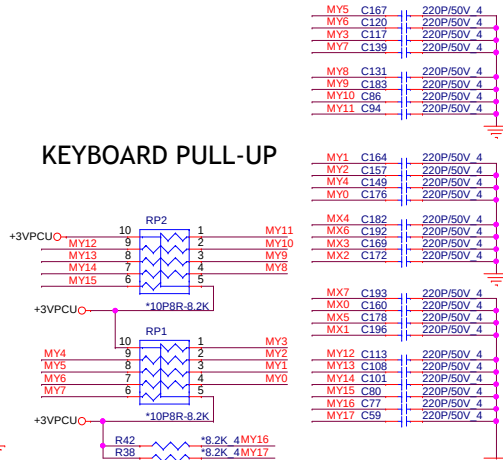
KEYBOARD Con.

26

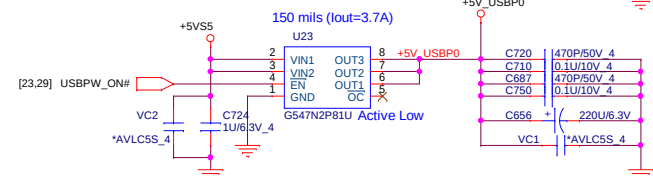
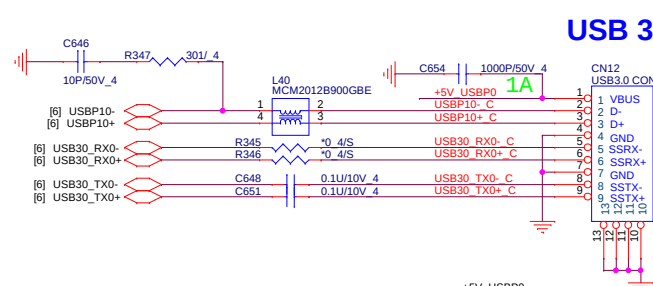
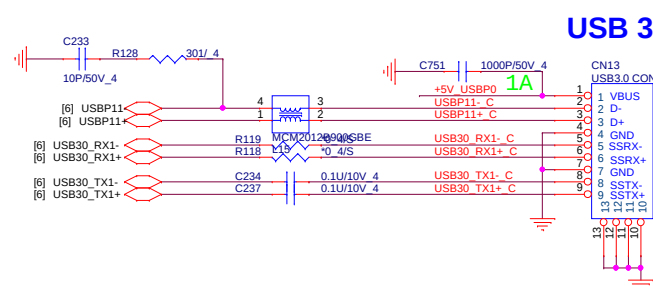
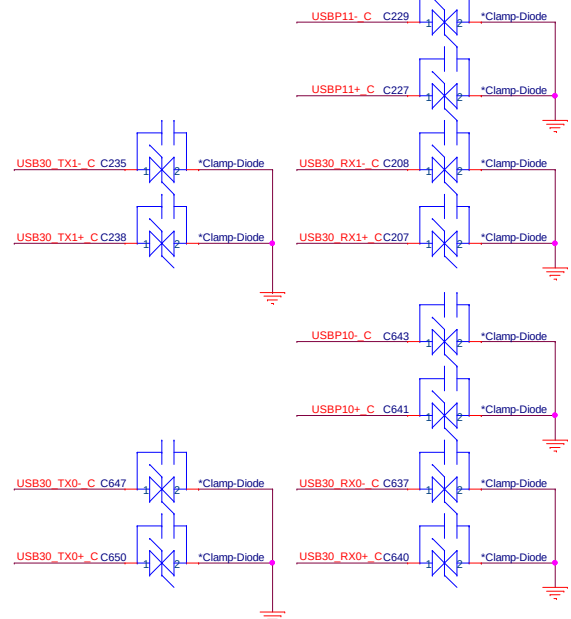


PV2 Change solution to same as U52

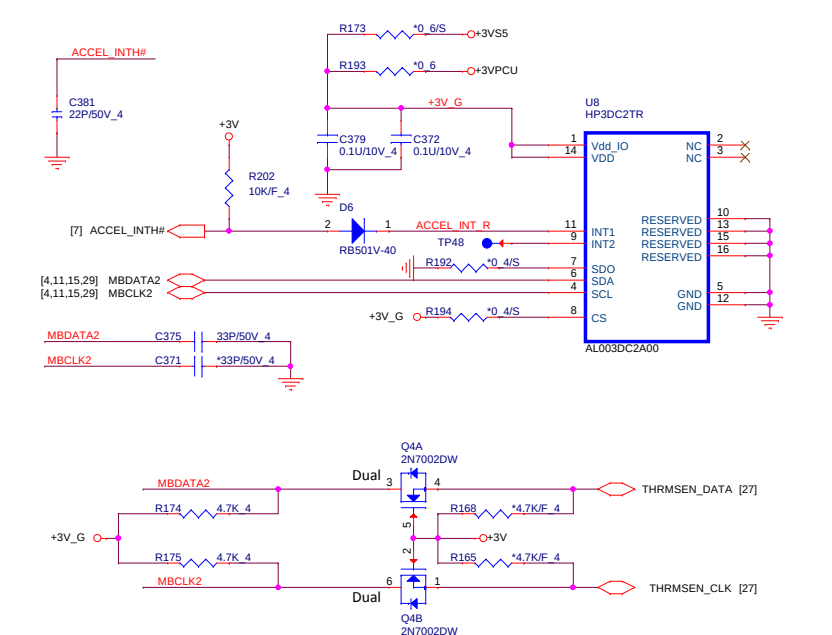
KEYBOARD PULL-UP



USB 2.0/3.0 Combo

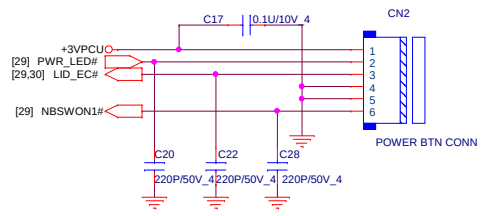


Accelerometer Sensor

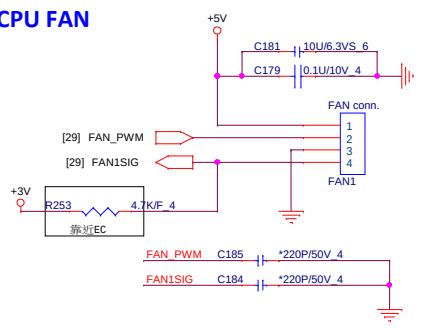


Power Button Connector

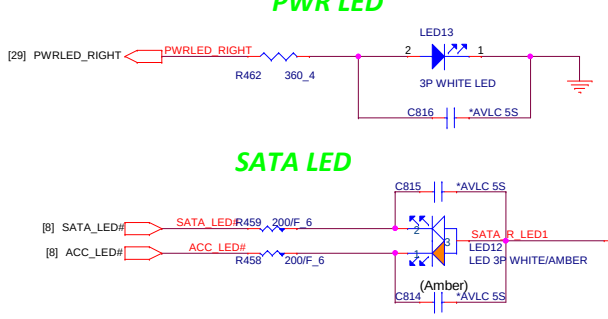
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



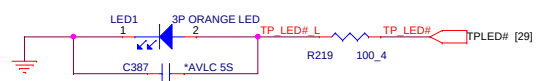
CPU FAN



LED Status

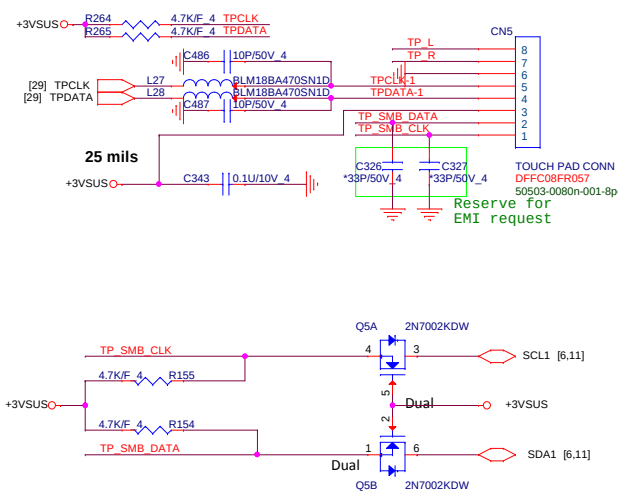
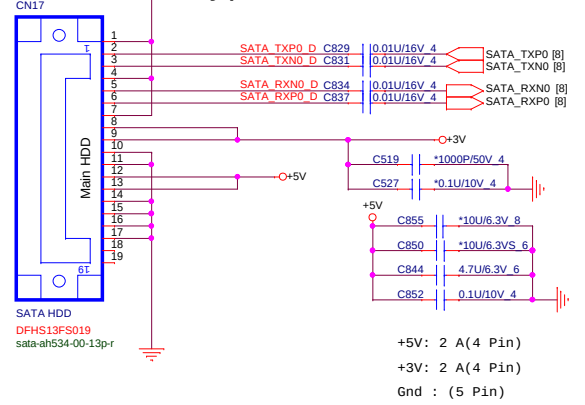


14 "TP LED

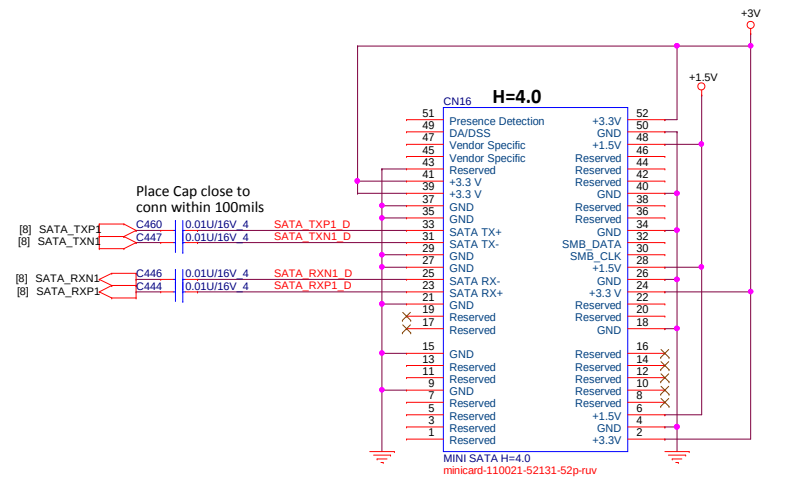


SATA HDD Connector(Cable type)

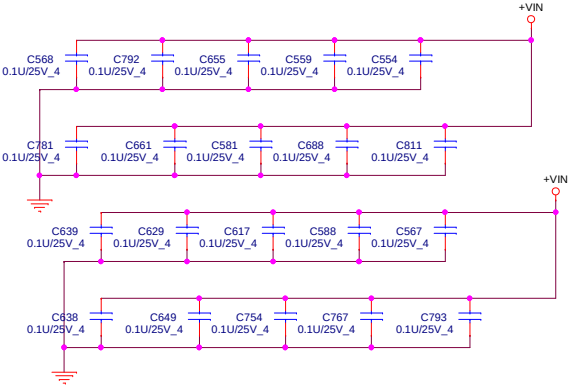
Bypass CAP c lose conn



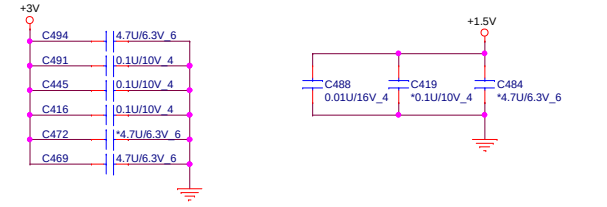
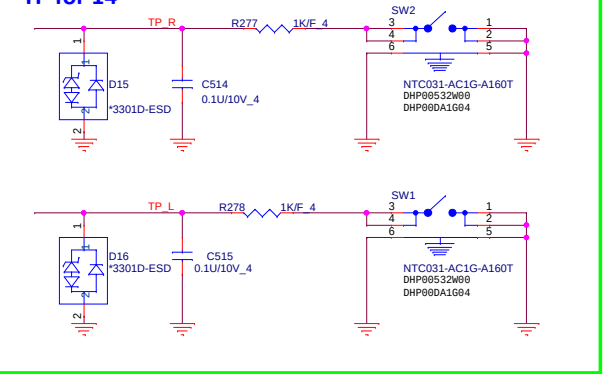
Mini PCI-E Card 2- Full size mSATA



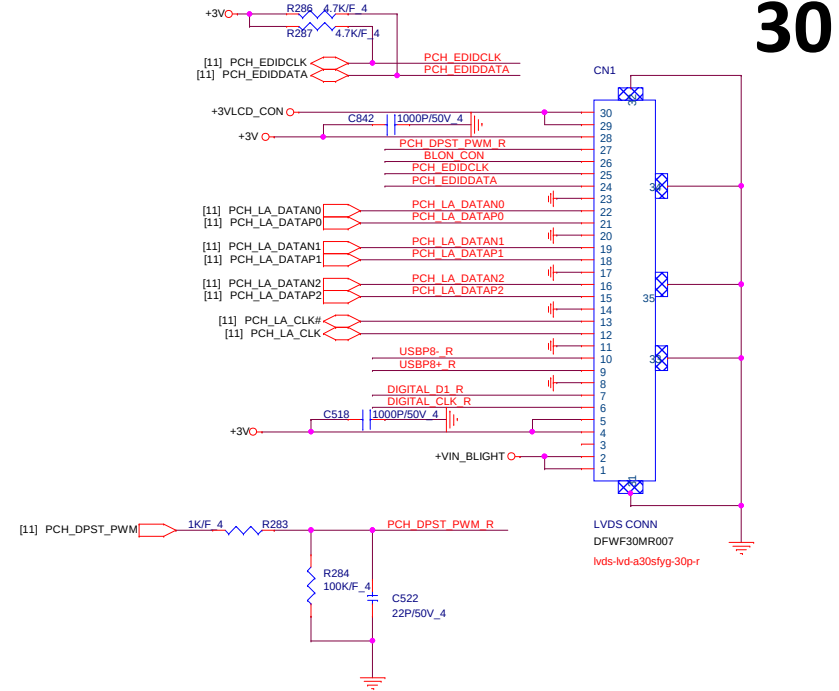
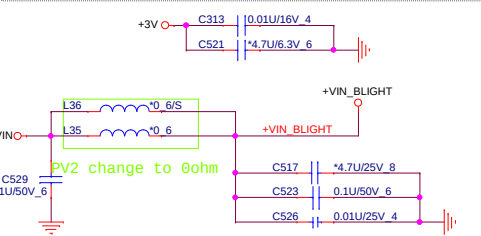
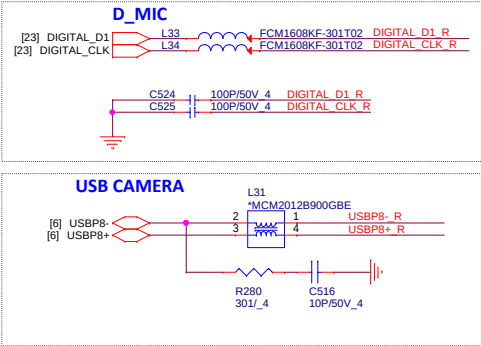
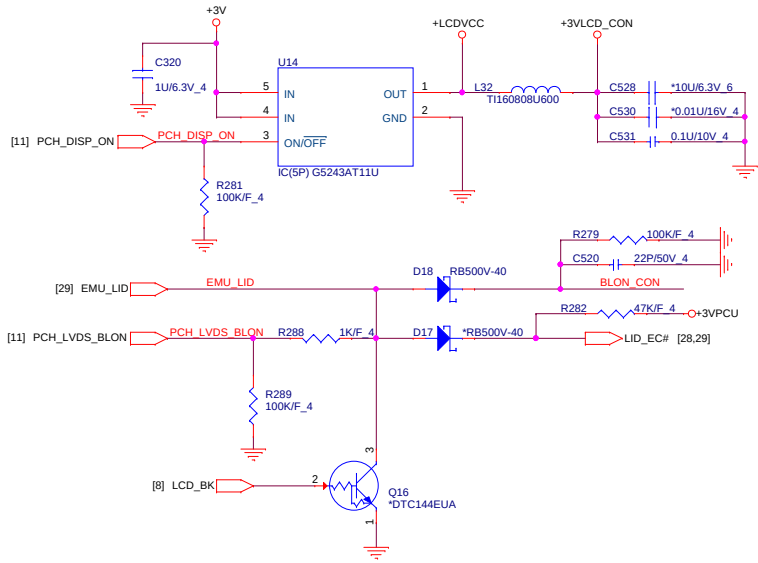
+VIN Cap



TP for 14"

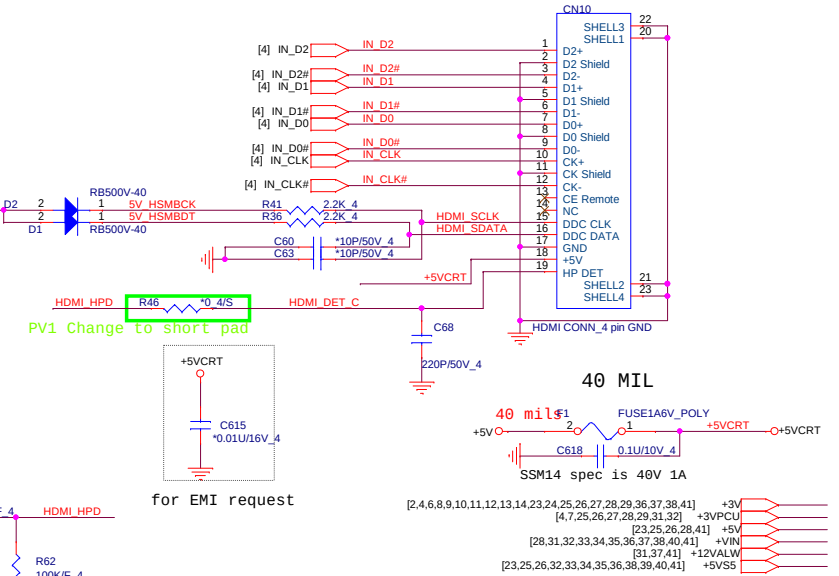
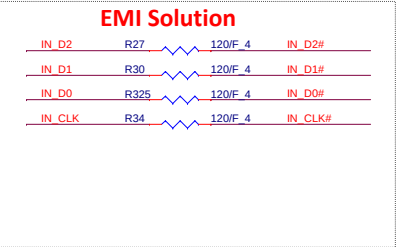
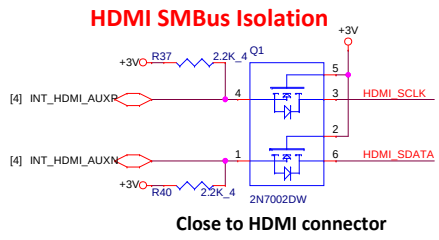


LVDS Conn.

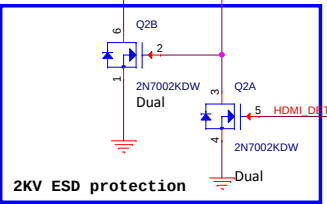


30

HDMI Conn.



HDMI HPD SENSE

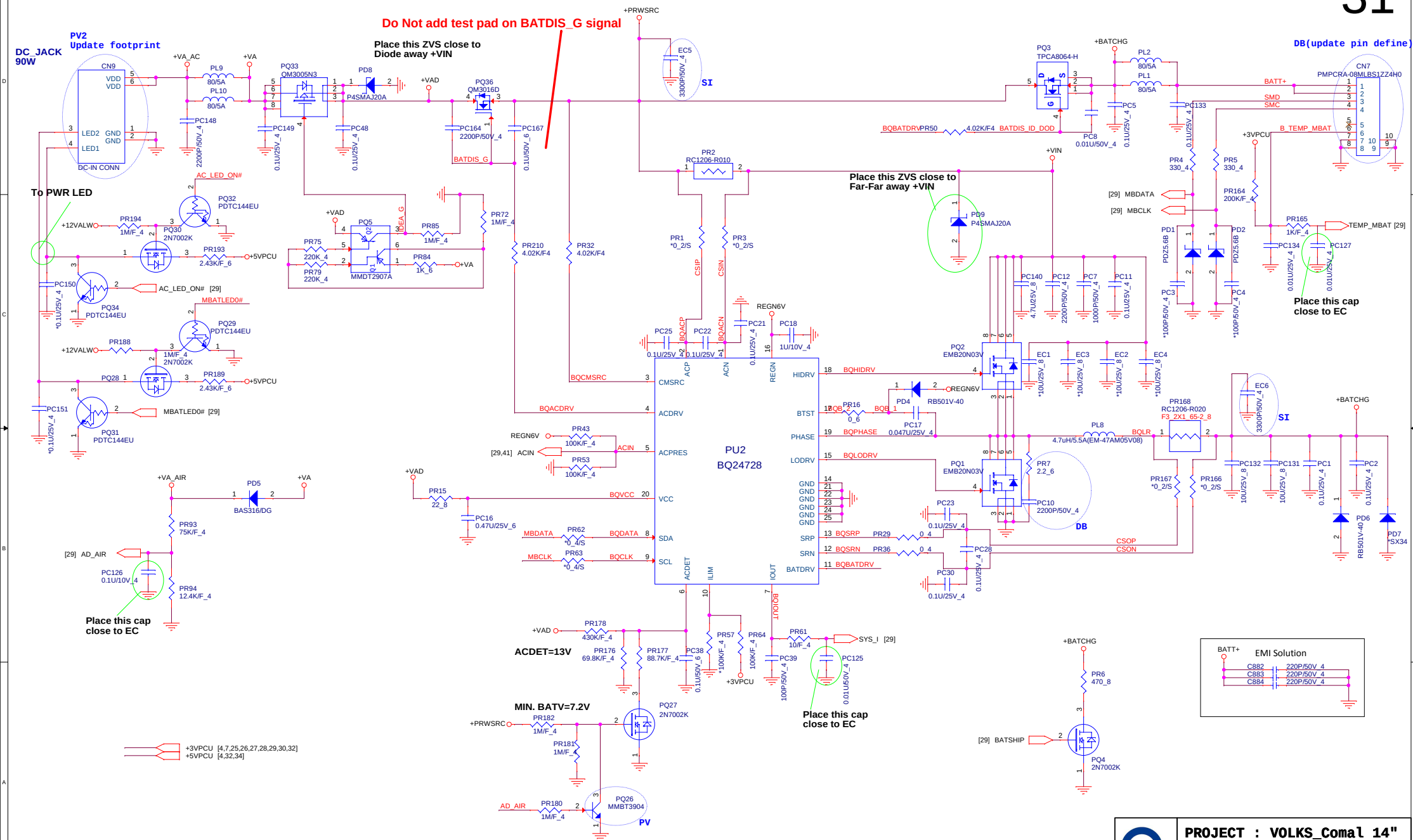




PROJECT : VOLKS Comal 14"
Quanta Computer Inc.

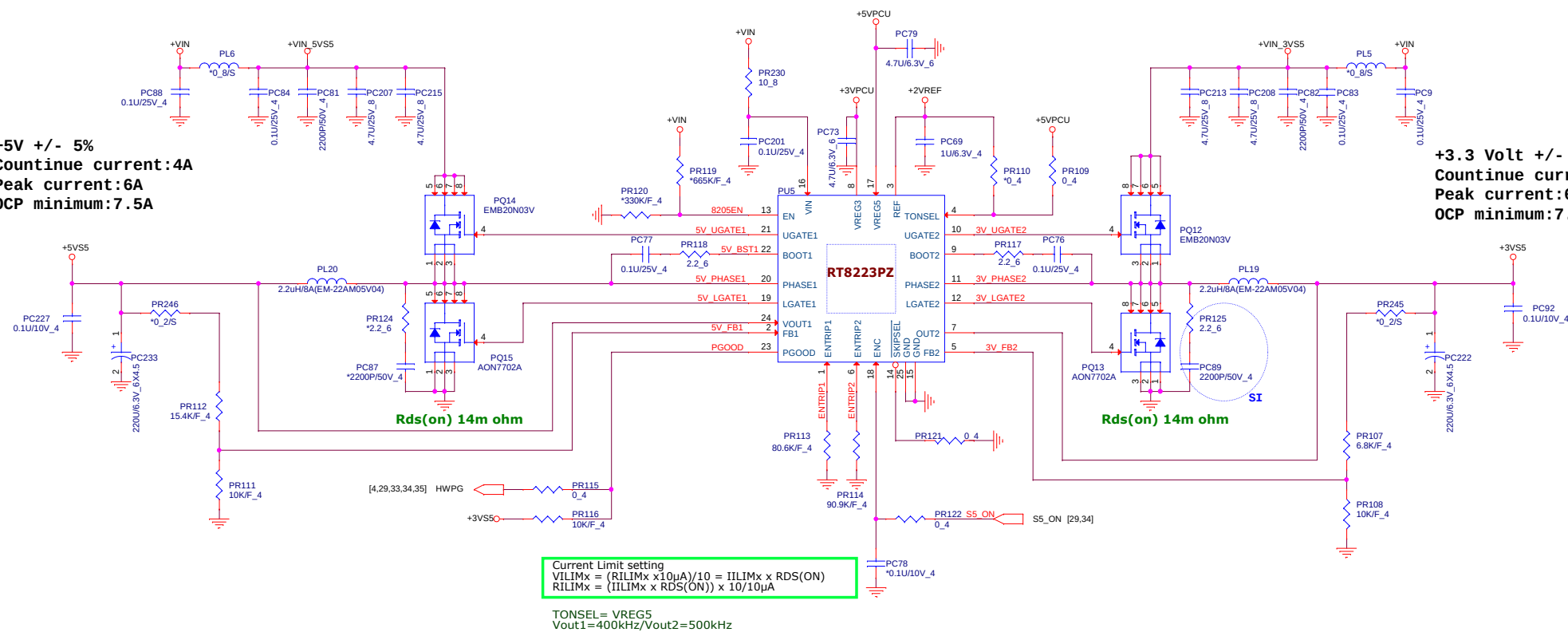
Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A

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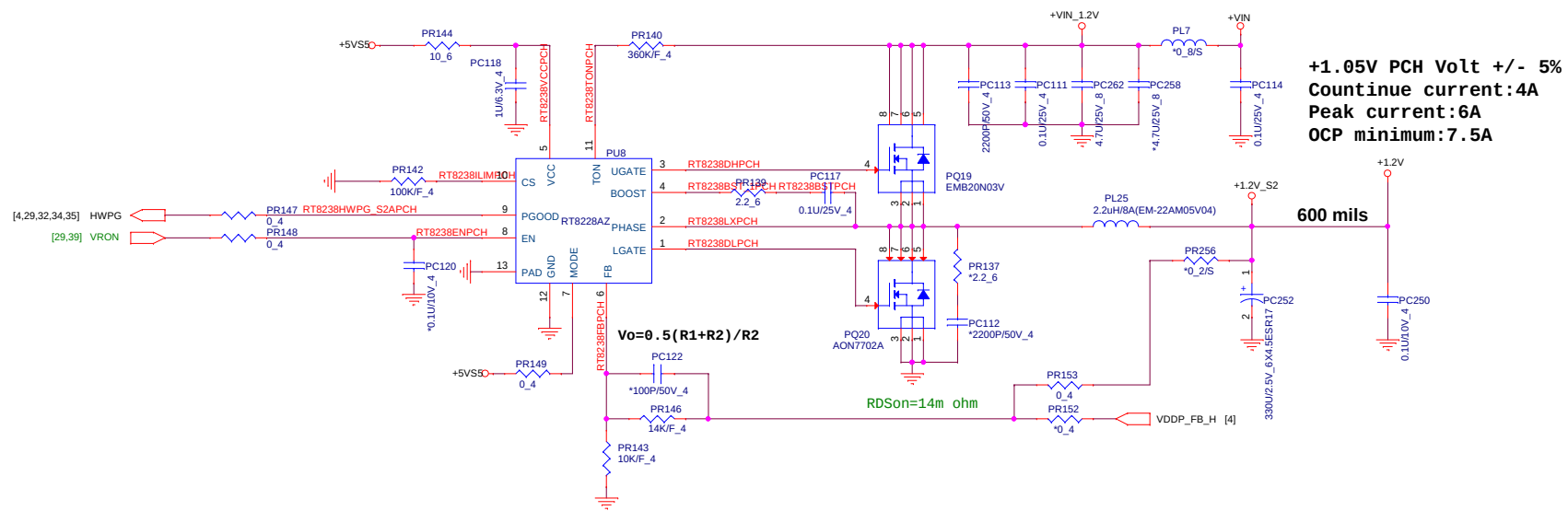


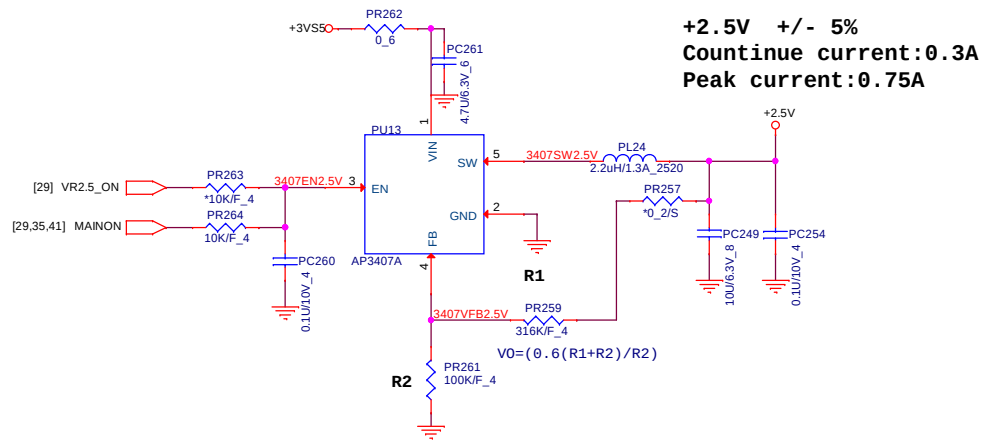
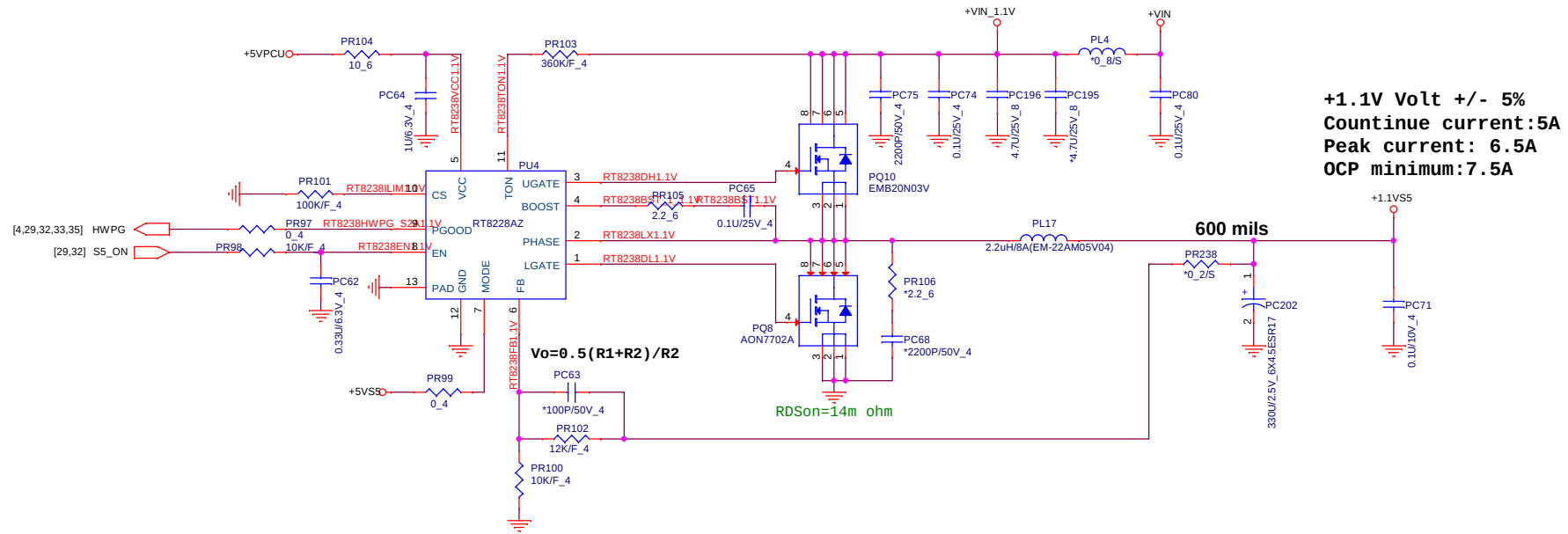
+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



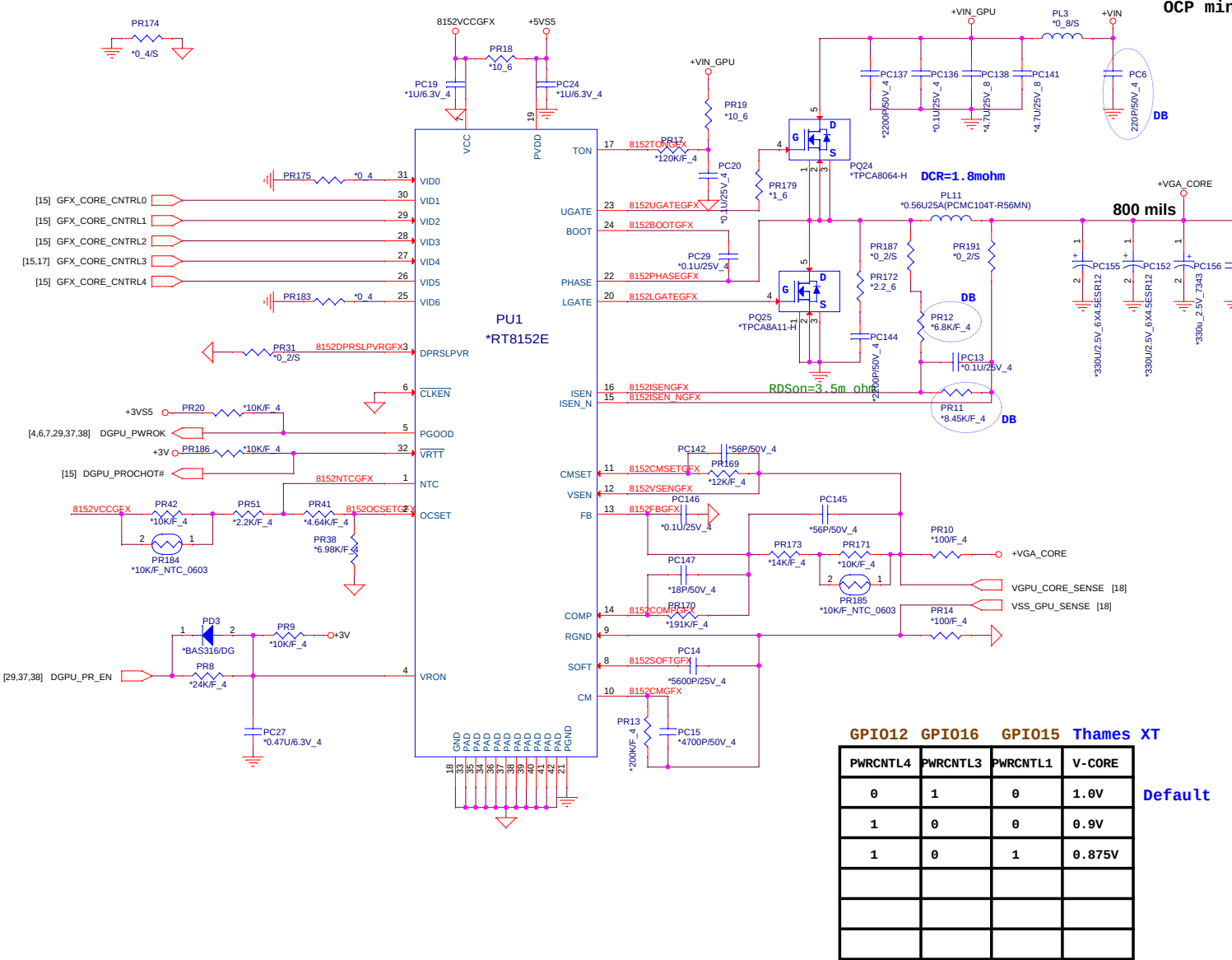
[28,30,31,33,34,35,36,37,38,40,41] +VIN
 [6,8,9,10,25,26,27,29,34,36,37,41] +3VSS
 [23,25,26,33,34,35,36,38,39,40,41] +5VSS
 [4,7,25,26,27,28,29,30,31] +3VPCU





VGA Core

+VGA_UMA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A



GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

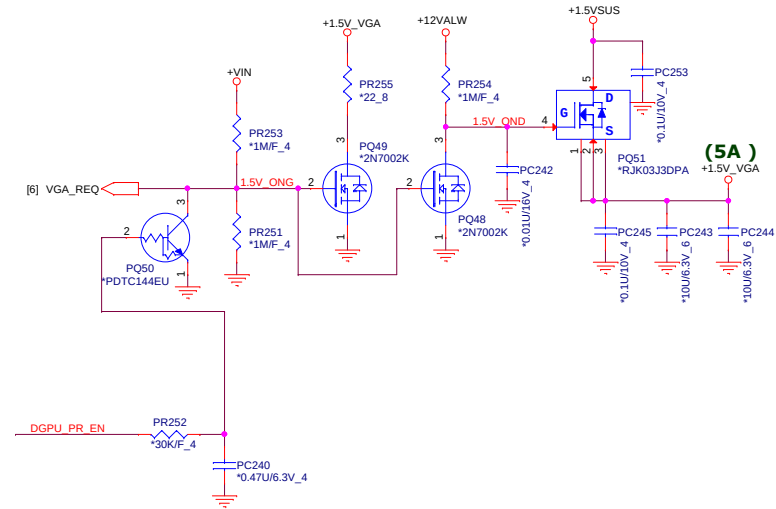
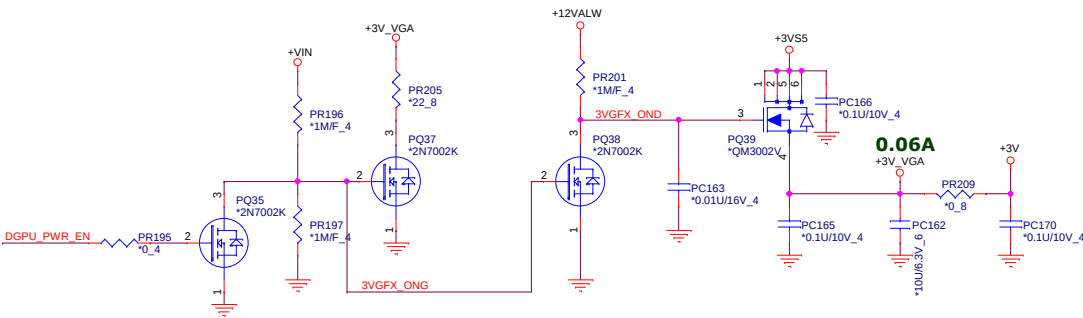
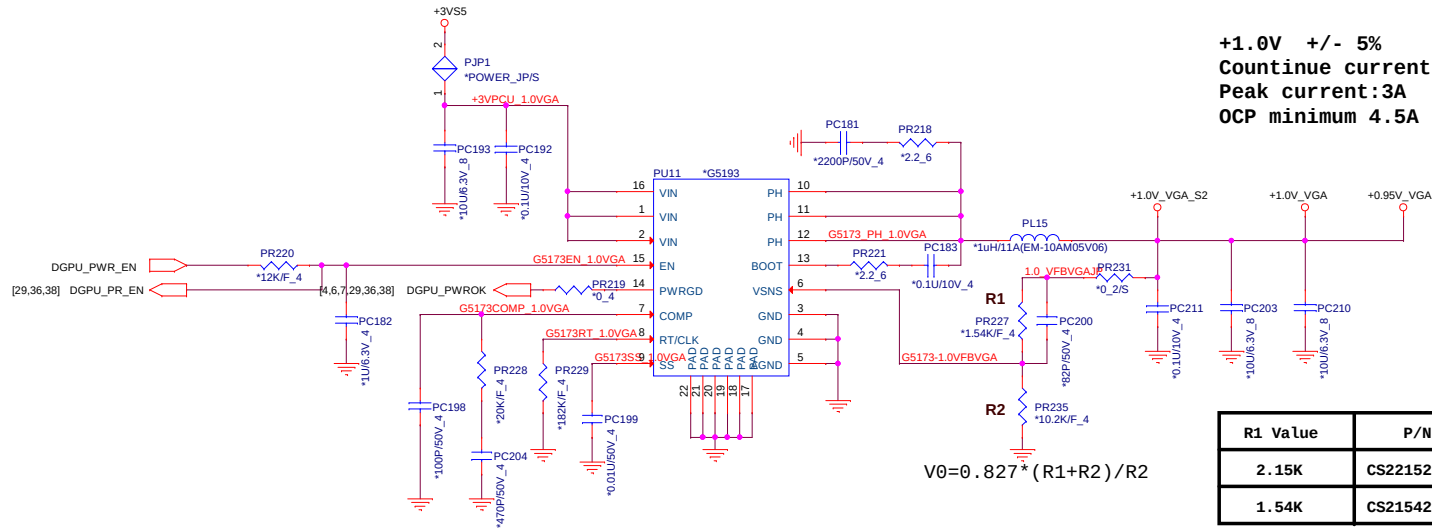
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

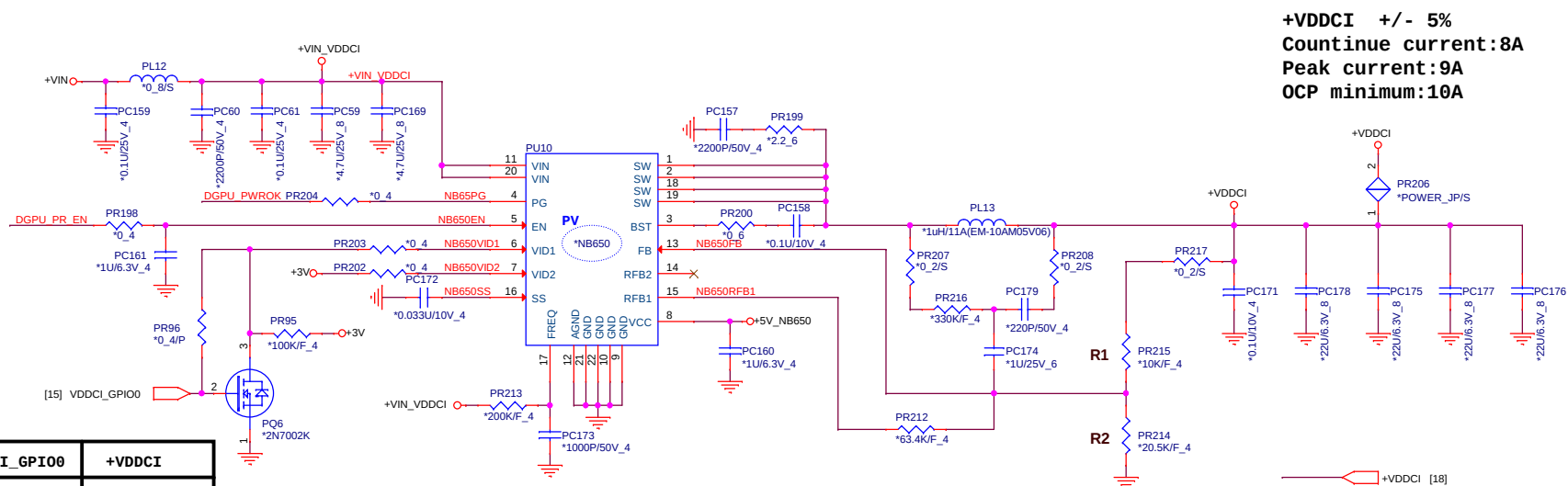
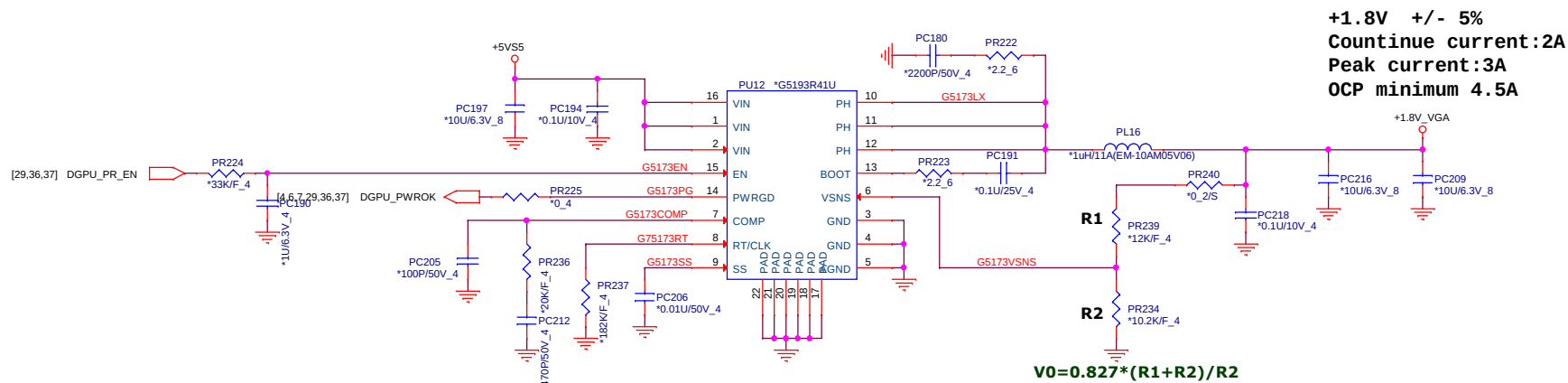
Default

GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

Default





VDDCI_GPI01	VDDCI_GPI00	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X



PROJECT : VOLKS_Coma1 14"
Quanta Computer Inc.

Size Custom	Document Number +1.8V_VGA (G5193)	Rev 1A
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